Chip-Package-System(CPS) Signal Integrity Co-Analysis

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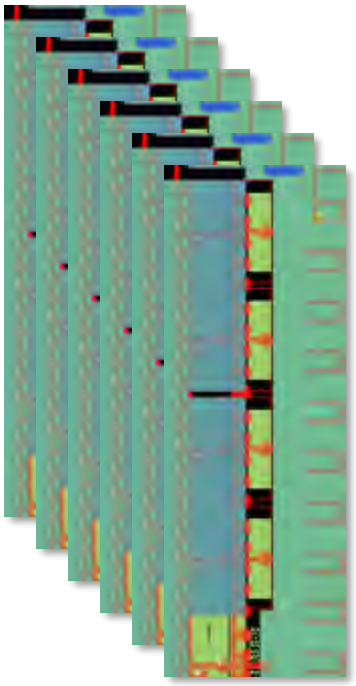
ANSYS

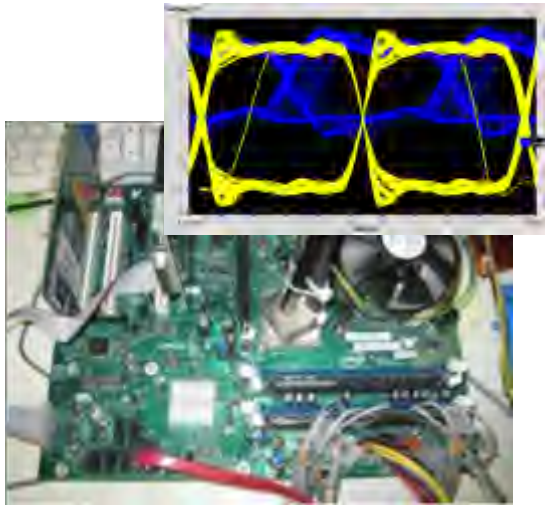
Agenda

- Traditional Industry Trend for Memory Interface Performance Check
- ANSYS Chip-Package-System Signal Integrity Solutions
- Detail Flow Demonstration based on DDR Design

Traditional Performance Check of DDRPHY Provider



Design multiple test IPs with required functions before mass production



Manufacturing & Measurement

- Select IP with the best performance
- No IP meeting target performance, needs tremendous effort for root-causing, fixing design

Late problem detection

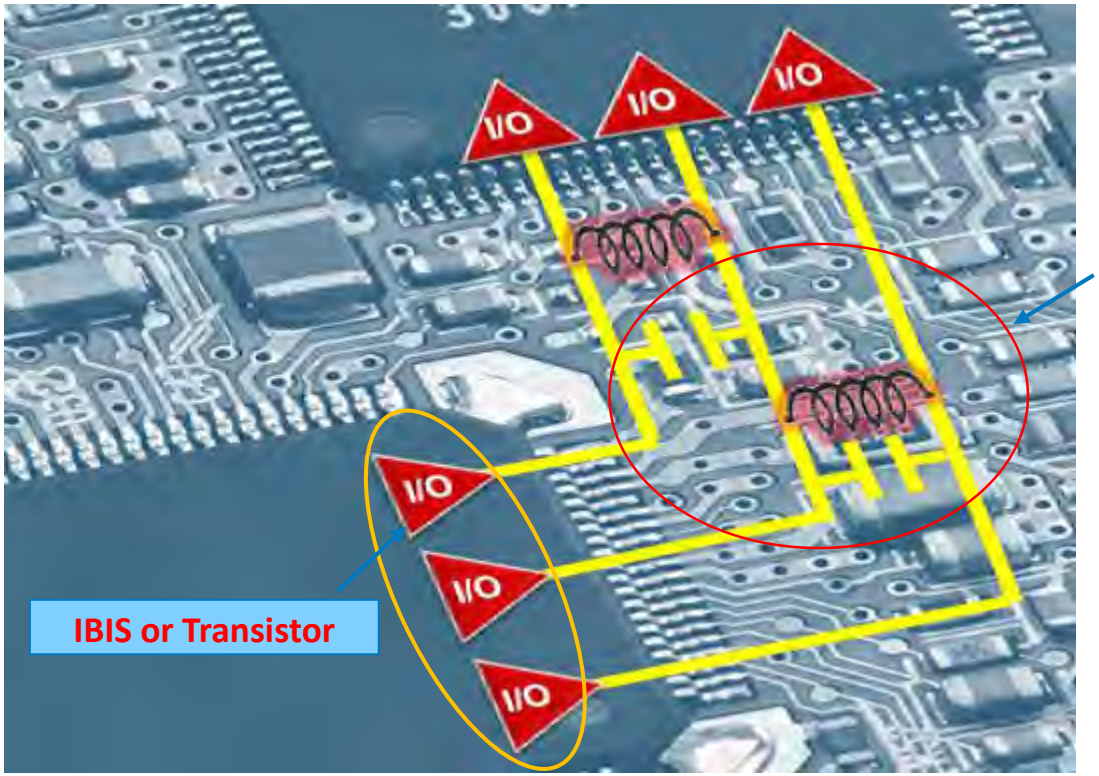
Cost Driven, Long TAT

The Higher Performance, the more difficult release products on time

Shadow area to SoC chip maker using 3rd part DDRPHY

Simulation based Performance Checking Solution is necessary

Traditional System Level Signal Integrity



- Direct connection btw IO and PKG without on-die PDN
- Generally consider only signal networks on package
- Can't consider power-to-signal coupling
  Power supply noise induced delay

Accuracy Loss due to insufficient data, high probability of under design

Traditional IO Model for DDR Timing Analysis

Constant delay model

Independent of supply voltage

Glitch, non-convergence

Most Accurate

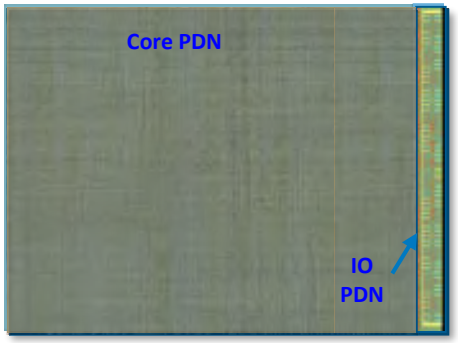
Can't full bank analysis due to capacity

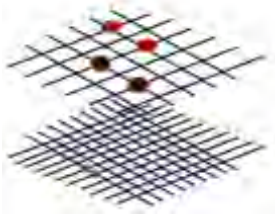
Greatly longer simulation time

Ideal Chip Model is

- *Faster than transistor*
- *Full Bank Capacity*
- *As accurate as transistor*
- *Including IO circuit function and intrinsic parasitic inside IO circuit*
- *Including Chip Layout(IO/Core PDN), IO decap cell*

Chip Signal Model(CSM) for DDR Timing Analysis





Including RDL, on-die de-caps

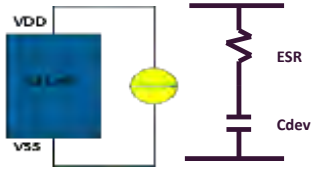
Multiple power domains

Per pad/bump broadband model

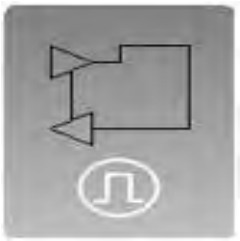
Compact model enables fast simulation in spice

CIOM(Chip IO Model)

- **Non-linear device I/O buffer macro-model**
- **Spice-level accuracy with full I/O bank capacity**
- **Captures impact of P/G noise on signal**
- **Load independent**
- **Layout and circuit IP encryption**
- **Also IBIS 5.0 Generation available**



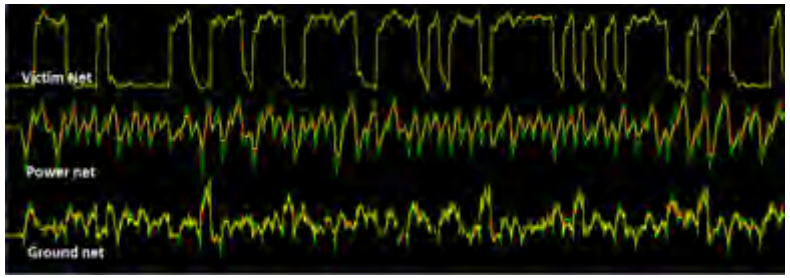
Intrinsic capacitance extraction of IO Cell



Chip Signal Model

Performance of CIOM and CSM

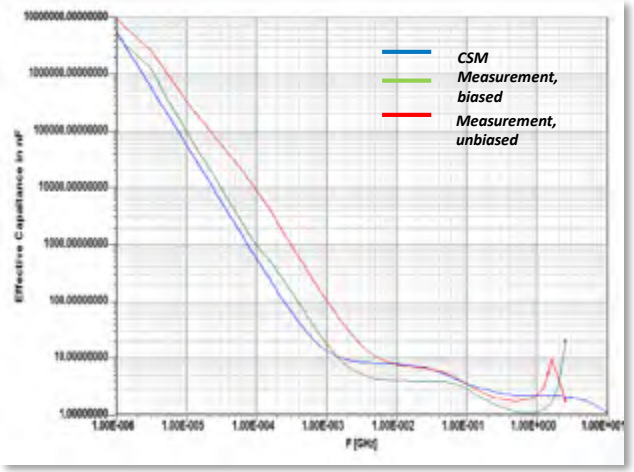
Comparison Xtor vs. CIOM vs. IBIS



	Run Time	VDD Swing (V)	# Nodes
All-Transistor	3hr 20min	0.24	1021805
All-CIOM	**12min**	**0.239**	**9597**
Transistors + IBIS	1hr 7min	0.38	160073

CIOM enables faster and accurate analysis!!

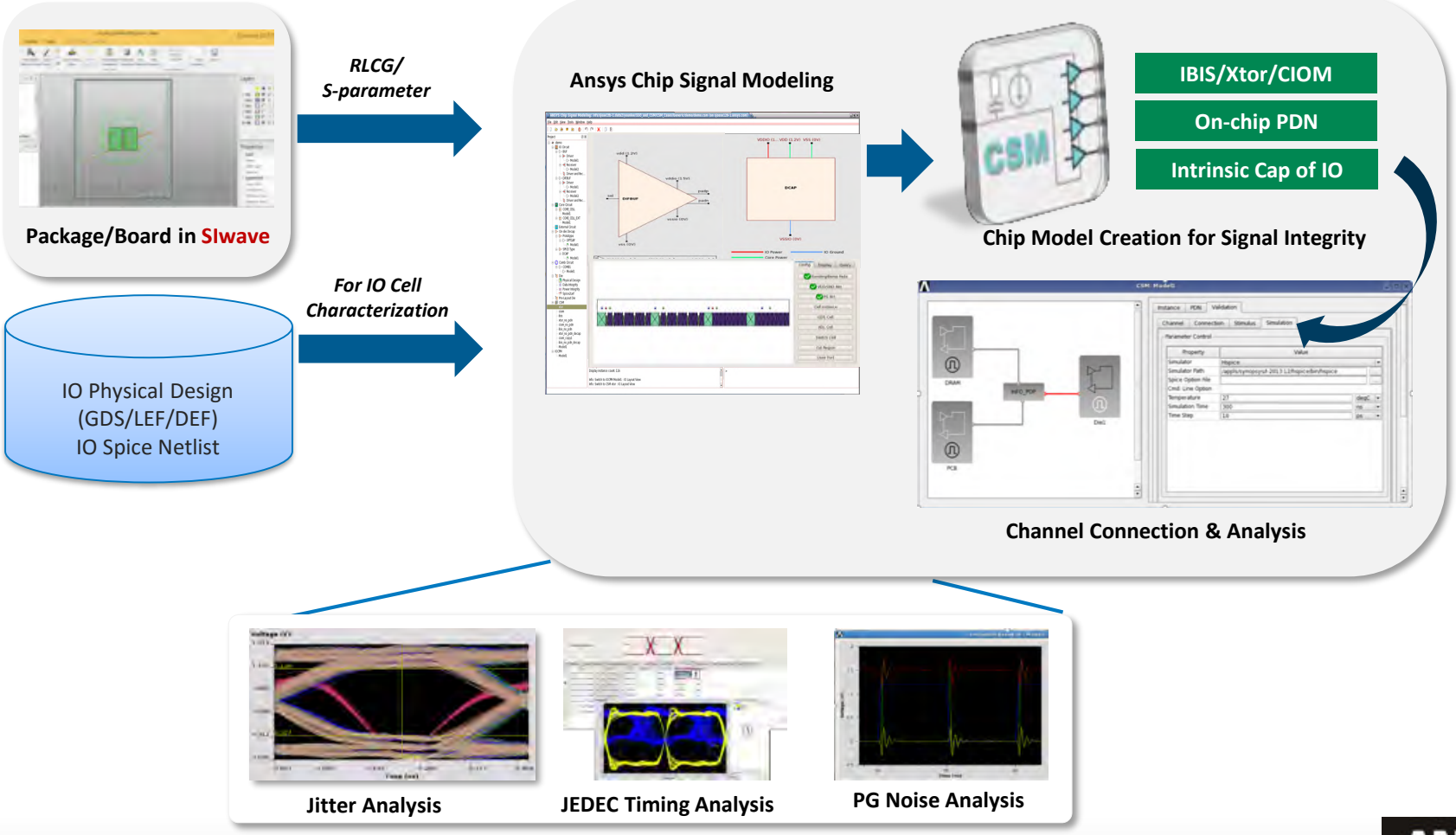
Correlation CSM vs. Measurement



CSM is well correlated with system level measurement

CPS Signal Integrity for Chip Designer

. Enables to predict power/signal Integrity performance check and optimization of DDRPHY
. This flow is feasible to package designer who can get chip design info



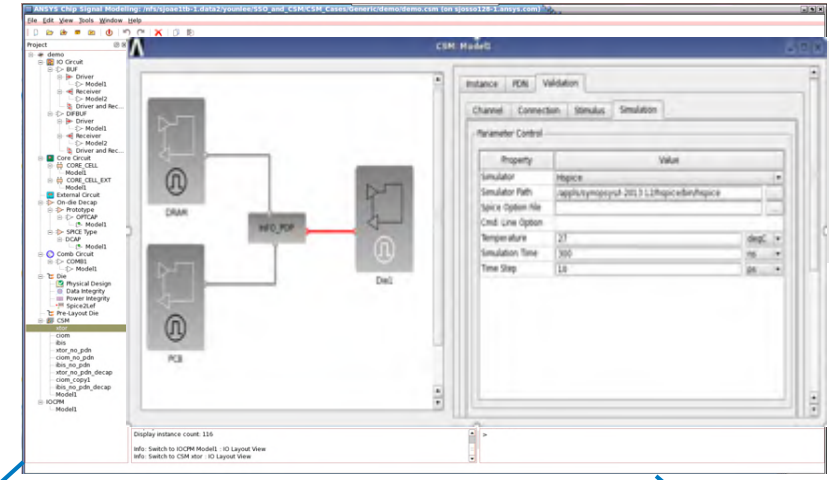
CPS Signal Integrity for Package Designer

. Enables package/system designer to do full bank PDN aware signal integrity analysis
. Prevent under/over design due to CSM which has all chip level info

Package/Board in SIwave

RLCG/
S-parameter

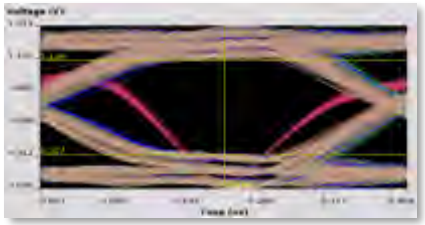
Ansys Chip Signal Modeling



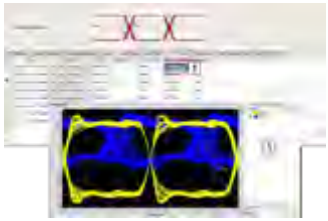
Channel Connection & Analysis

IBIS/Xtor/CIOM
On-chip PDN
Intrinsic Cap of IO

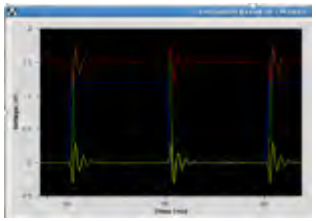
Chip Model Creation for Signal Integrity



Jitter Analysis



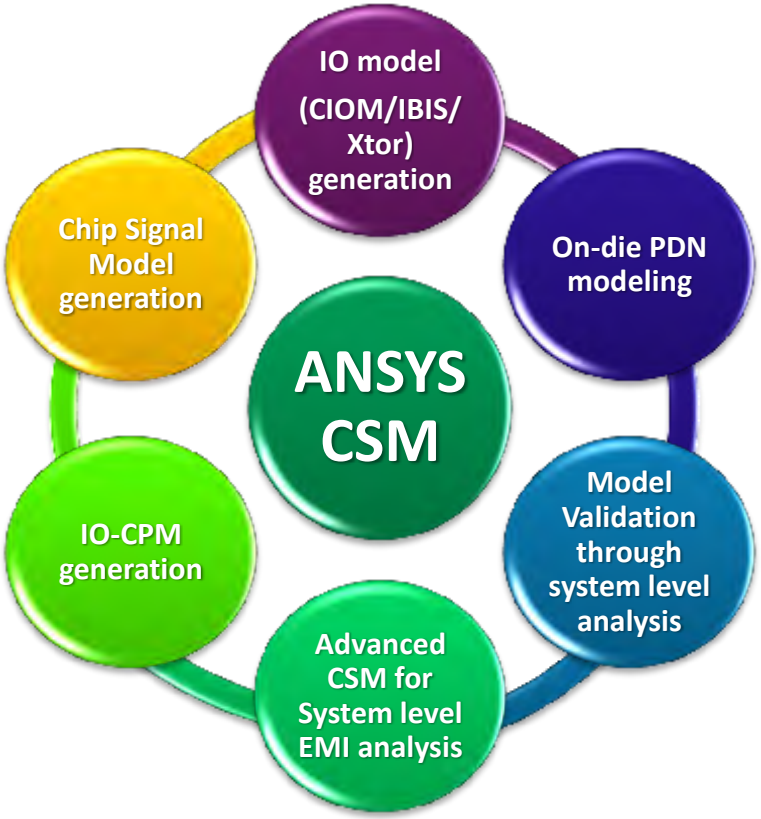
JEDEC Timing Analysis



PG Noise Analysis

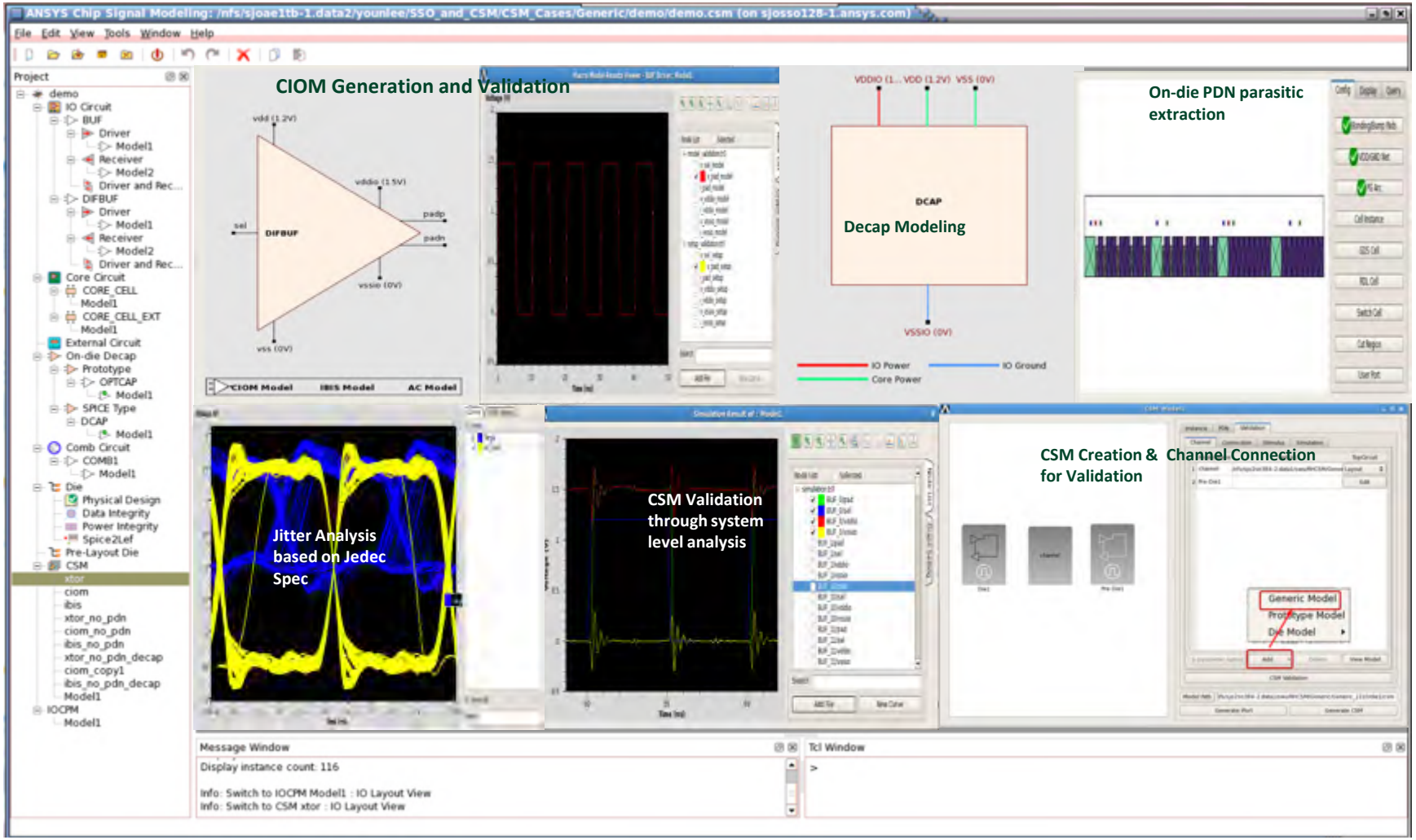
Demo Video: Extract Parasitic of Board PDN via SIwave-CPA

ANSYS Chip Signal Modeling

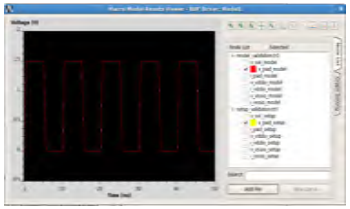


- Chip Model generation for DDR timing and EMI
- Chip & System level signal Integrity simulation
- Target User: Package designer, Chip DDRPHY or IO designer
- Validation includes JEDEC compatible timing, noise, jitter, slew reporting covering single ended and differential type IOs
- Customized 3DIC, HBM, WLP(Wafer Level Package) target CSM generation & validation

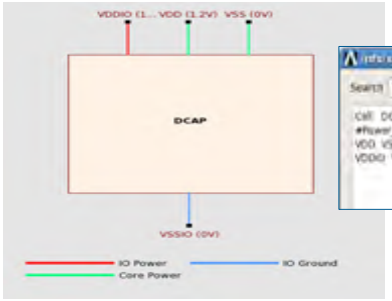
ANSYS CSM GUI Overview

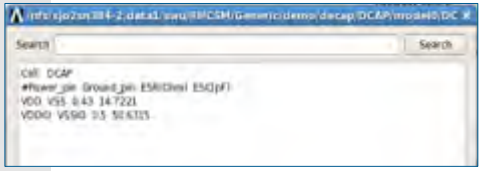


Chip Signal Model Creation and Validation Flow

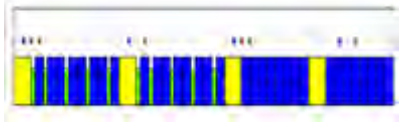



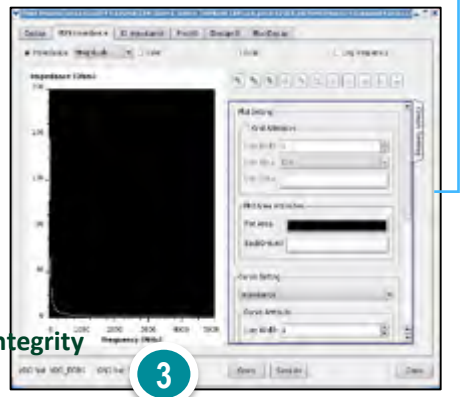
1 CIOM Generation and Validation



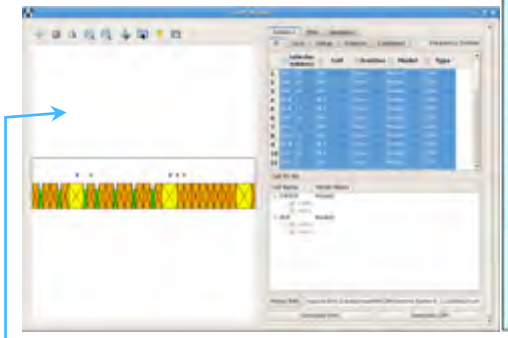


IO Decap Modeling 2

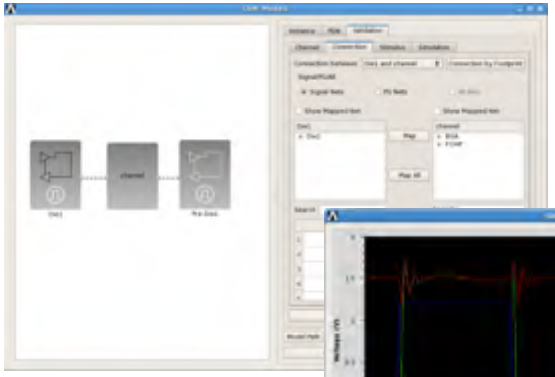
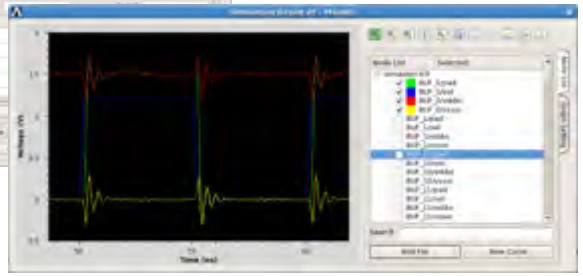




3 Parasitic Extraction and Power Integrity Analysis of on-chip PDN

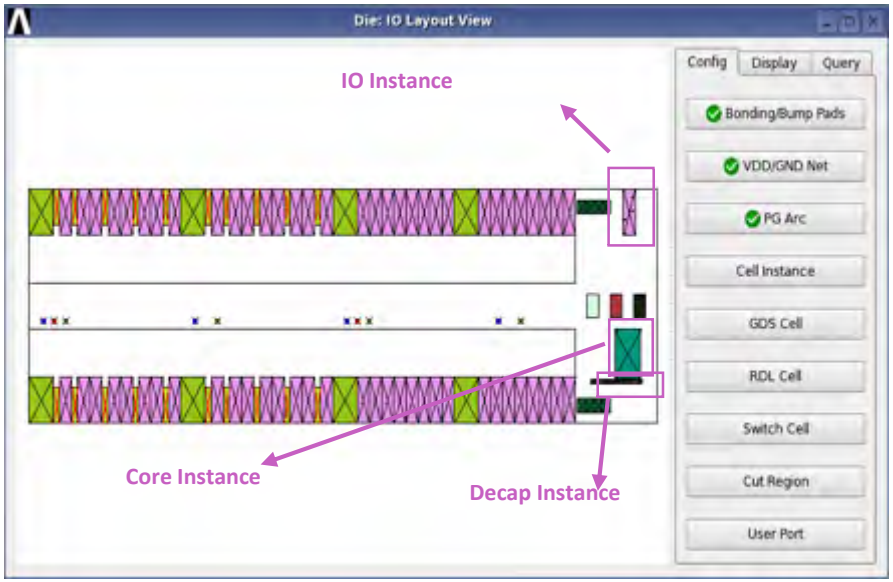



CSM(Chip Signal Model) Creation 4

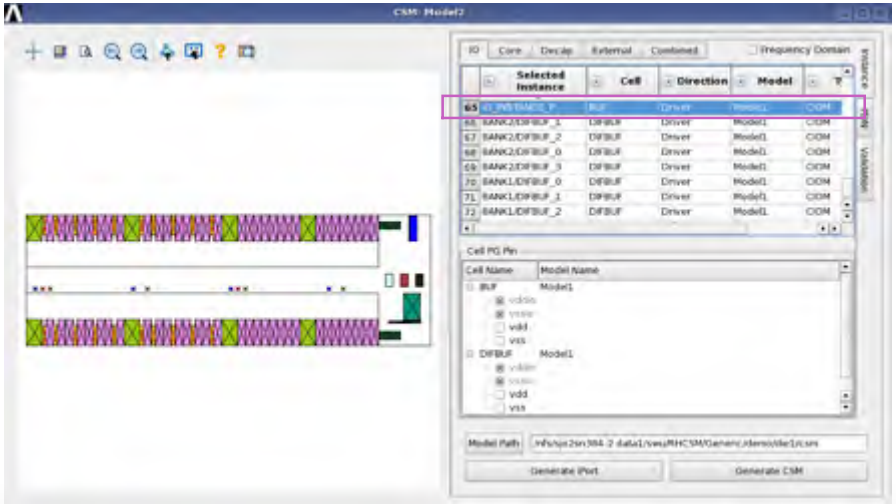



Simulation env. set up for CSM validation 5

What-if analysis for DDRPHY IO/Decap Optimization



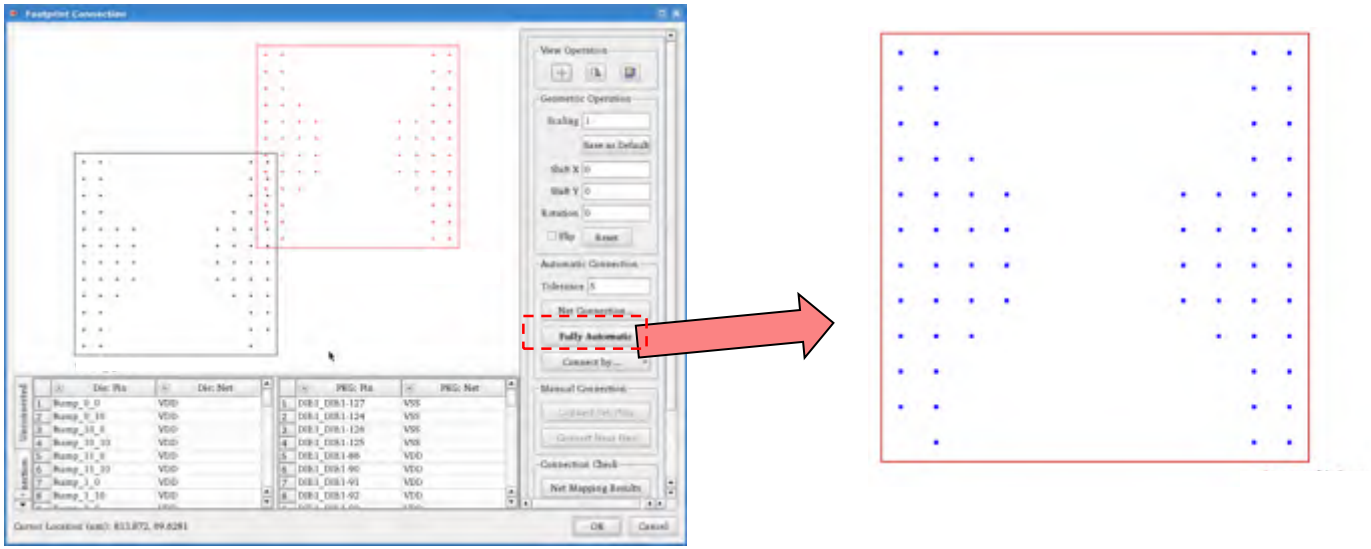
- IO/Decap/Core Instance can be newly defined or added;
- User-defined cell instances are placed in DDRPHY.



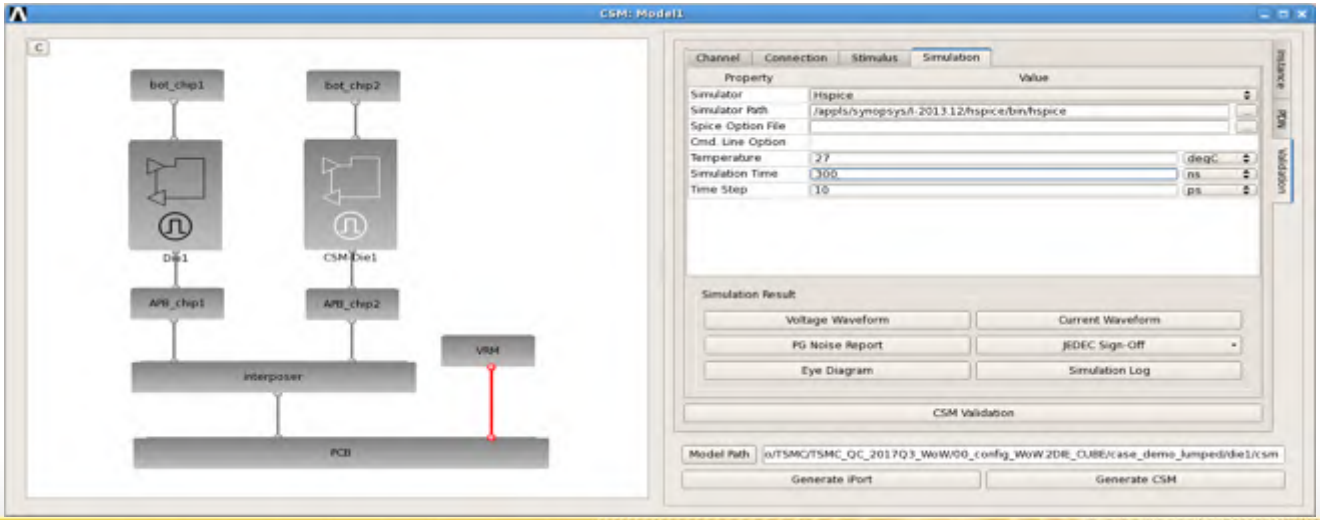
- Enables to generate various types of CSM with different optimization case;
- User can do performance check through channel simulation and select the best case.

Demon Video: CSM Model Creation of DDR Design

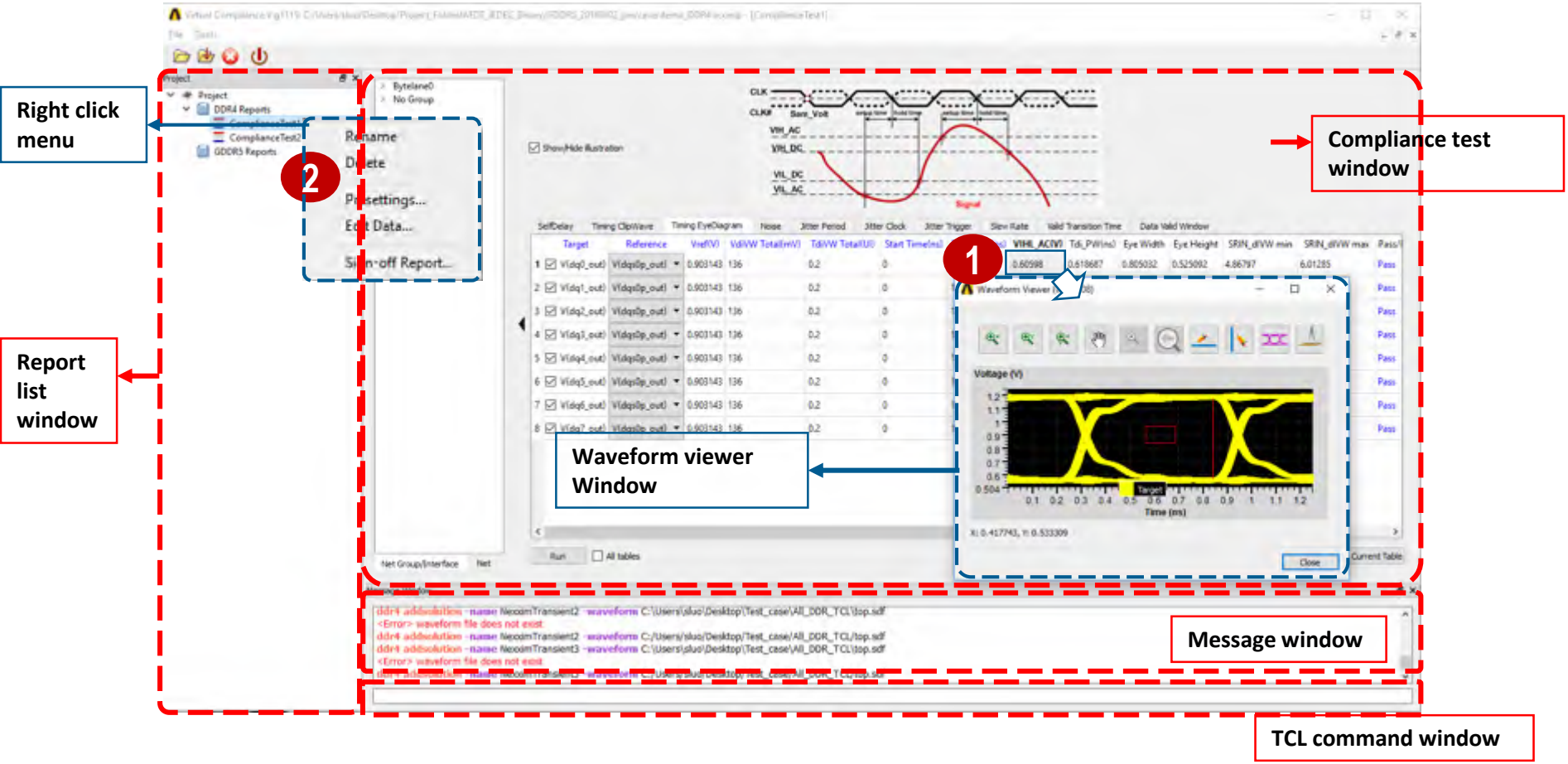
Channel Connection & Auto Simulation Test bench Creation



CSM and all parasitic models from SIwave enables auto electrical connection between driver dies, Package and Board to receiver through CPP(Chip Package Protocol) header

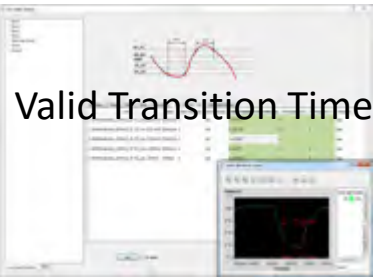


New Virtual Compliance GUI Overview

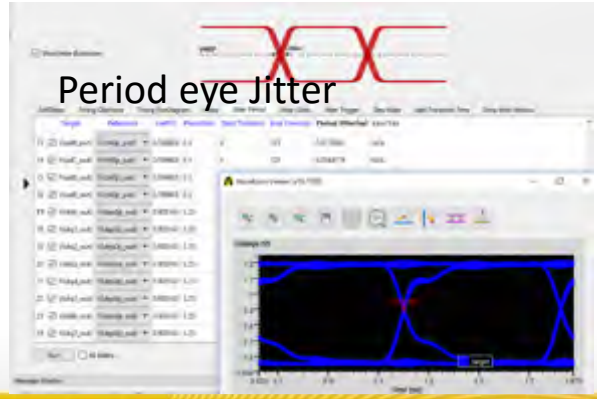


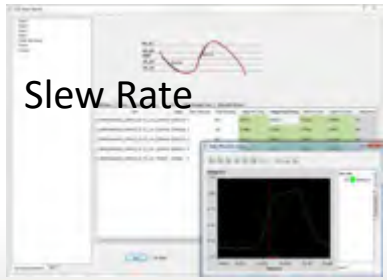
1. Each report cell can pop-up a waveform viewer window
2. Right click menu can export HTML format report.

Reporting Tables Overview

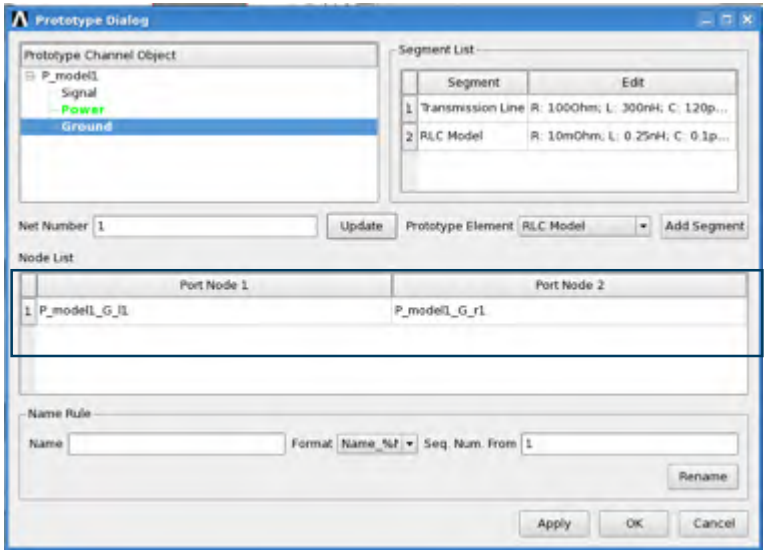


Virtual Compliance Toolkit



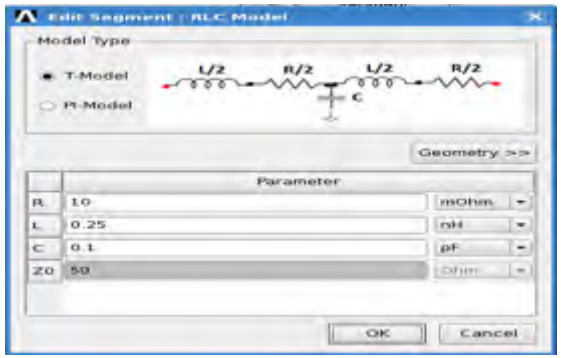


Prototype Package & Board Channel Model

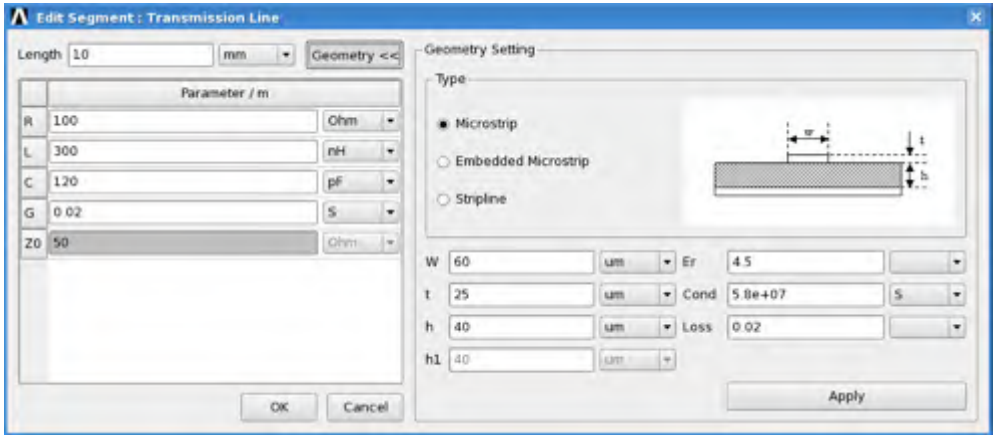


- Enables to predict performance check at the early design stage
- Instantaneous impedance(Z0) is auto decided by RLC in the RLC Model
- RLC & Z0 have been generated by geometry define in the Transmission Line Model
- As for multiple channel, mutual coupling effects can be defined between channels

RLC Model



Transmission Line



Demonstration Video

感谢聆听