

ANSYS



仿真
新时代

2017 ANSYS用户技术大会

中国·烟台

Chip-Package-System(CPS) Signal Integrity Co-Analysis

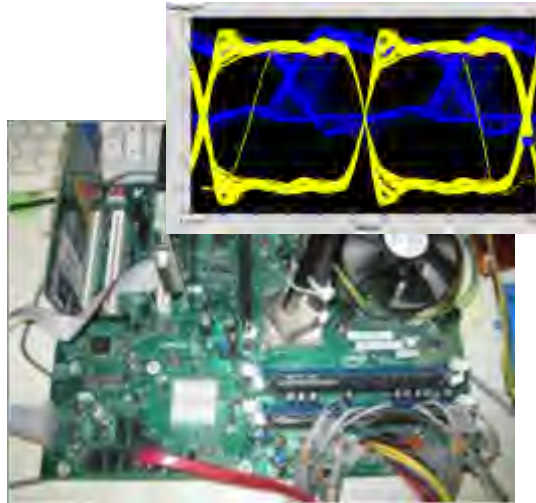
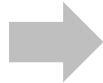
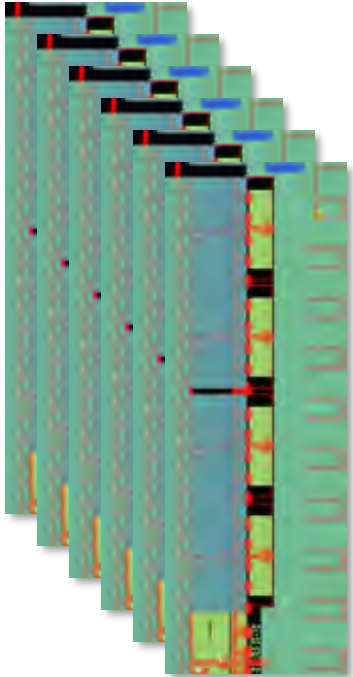
Rodger Luo / Sr. Product Engineer

ANSYS

Agenda

- **Traditional Industry Trend for Memory Interface Performance Check**
- **ANSYS Chip-Package-System Signal Integrity Solutions**
- **Detail Flow Demonstration based on DDR Design**

Traditional Performance Check of DDRPHY Provider



Manufacturing & Measurement

- Select IP with the best performance
- No IP meeting target performance, needs tremendous effort for root-causing, fixing design

Late problem detection

Cost Driven, Long TAT

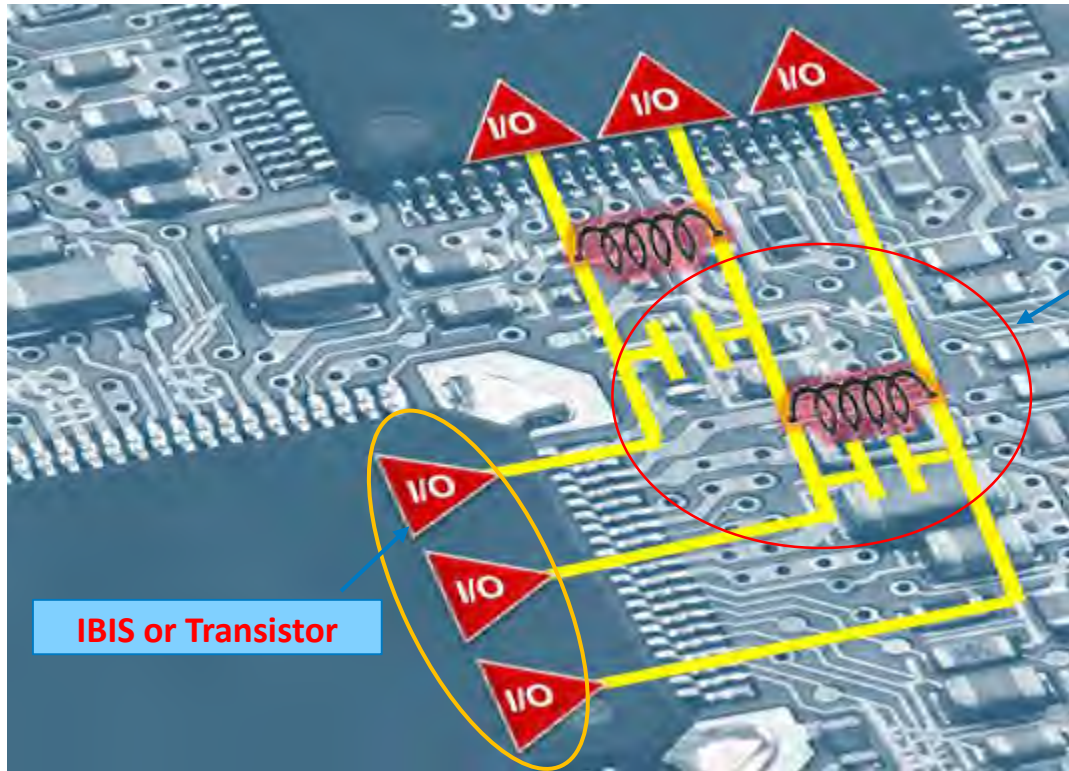
Design multiple test IPs with required functions before mass production

The Higher Performance, the more difficult release products on time

Shadow area to SoC chip maker using 3rd part DDRPHY

Simulation based Performance Checking Solution is necessary

Traditional System Level Signal Integrity



- Direct connection btw IO and PKG without on-die PDN
- Generally consider only signal networks on package
- Can't consider power-to-signal coupling
Power supply noise induced delay

Accuracy Loss due to insufficient data, high probability of under design

Traditional IO Model for DDR Timing Analysis

Constant delay model



Independent of supply voltage

Glitch, non-convergence

Most Accurate



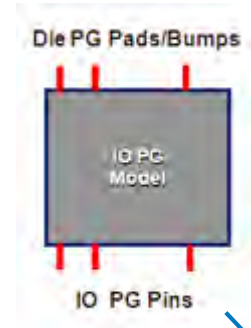
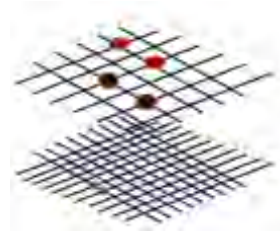
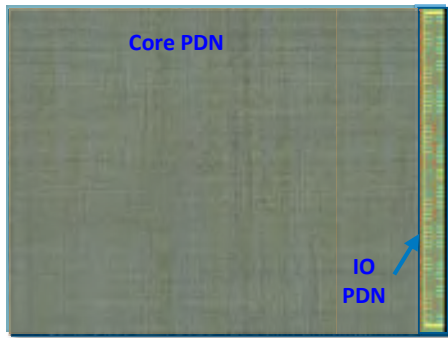
Can't full bank analysis due to capacity

Greatly longer simulation time

Ideal Chip Model is

- *Faster than transistor*
- *Full Bank Capacity*
- *As accurate as transistor*
- *Including IO circuit function and intrinsic parasitic inside IO circuit*
- *Including Chip Layout(IO/Core PDN), IO decap cell*

Chip Signal Model(CSM) for DDR Timing Analysis

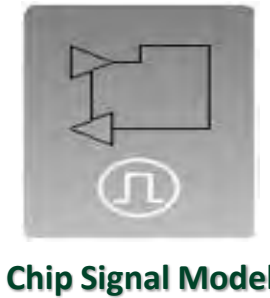
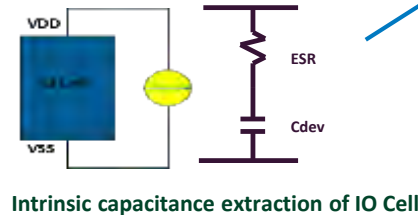


Including RDL, on-die de-caps
 Multiple power domains
 Per pad/bump broadband model
 Compact model enables fast simulation in spice



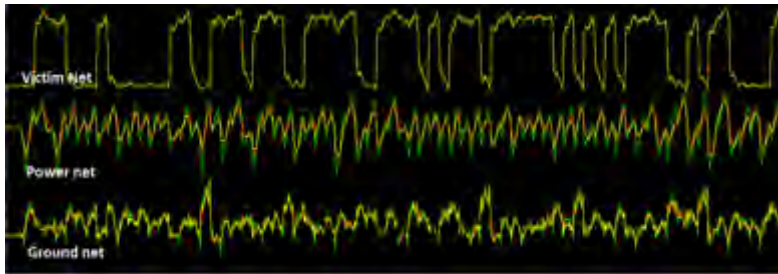
CIOM(Chip IO Model)

- Non-linear device I/O buffer macro-model
- Spice-level accuracy with full I/O bank capacity
- Captures impact of P/G noise on signal
- Load independent
- Layout and circuit IP encryption
- Also IBIS 5.0 Generation available



Performance of CIOM and CSM

Comparison Xtor vs. CIOM vs. IBIS

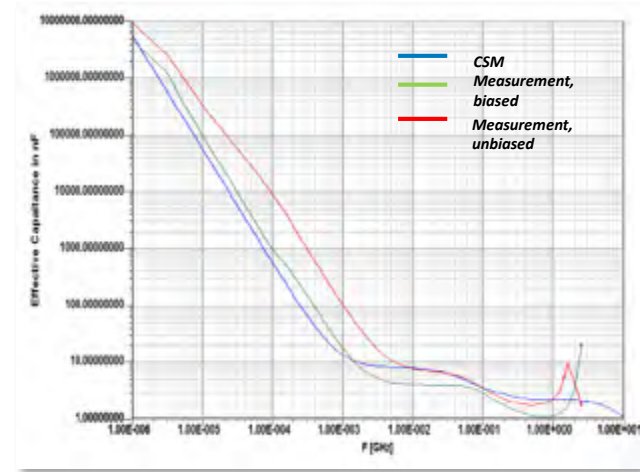


— 32bit All Transistor — 32bit All CIOM
 — 5 Transistor w/ 27bit IBIS power noise aggressor model

	Run Time	VDD Swing (V)	# Nodes
All-Transistor	3hr 20min	0.24	1021805
All-CIOM	12min	0.239	9597
Transistors + IBIS	1hr 7min	0.38	160073



Correlation CSM vs. Measurement

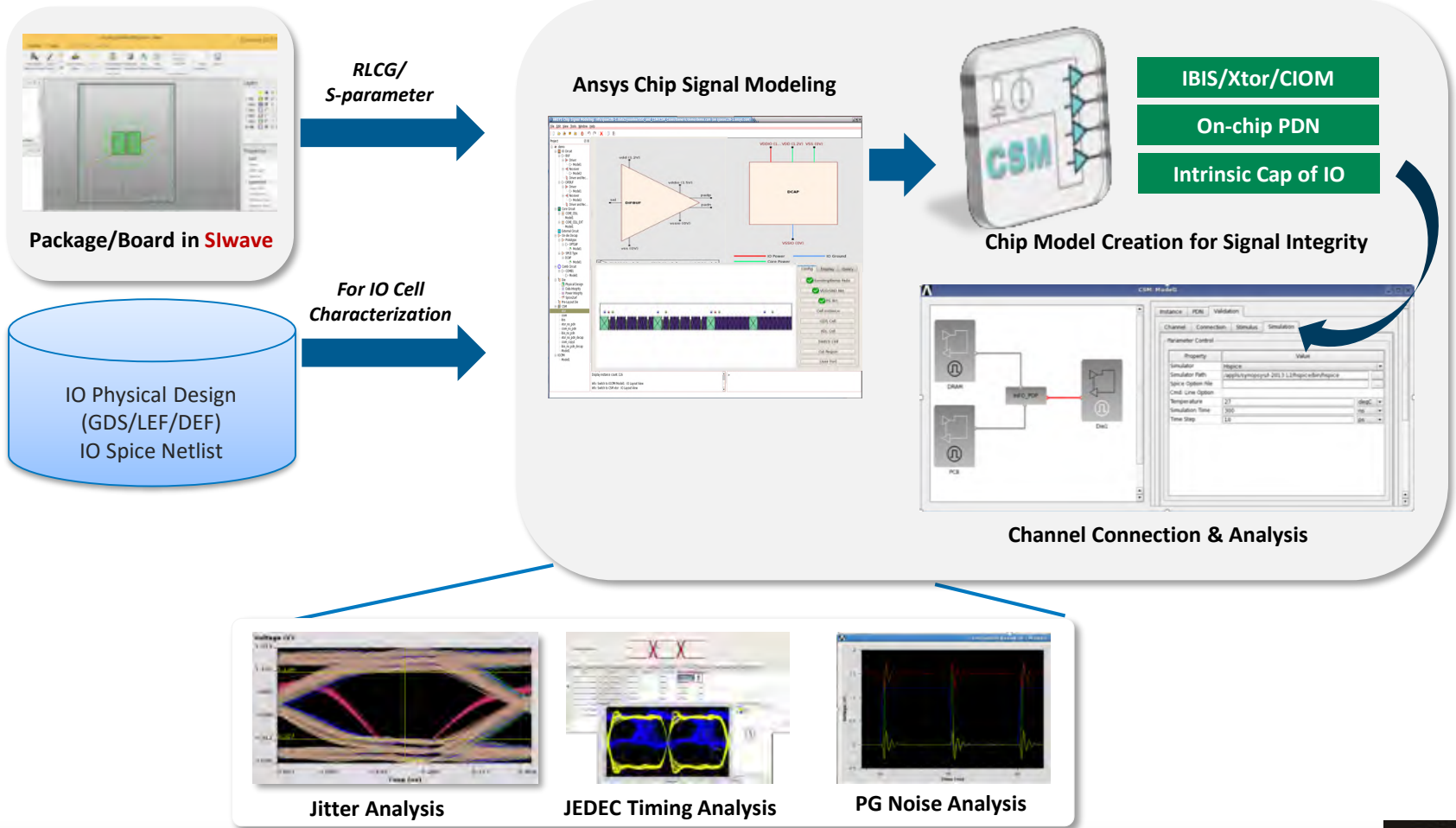


CSM is well correlated with system level measurement

CIOM enables faster and accurate analysis!!

CPS Signal Integrity for Chip Designer

- . Enables to predict power/signal Integrity performance check and optimization of DDRPHY
- . This flow is feasible to package designer who can get chip design info



CPS Signal Integrity for Package Designer

- . Enables package/system designer to do full bank PDN aware signal integrity analysis
- . Prevent under/over design due to CSM which has all chip level info



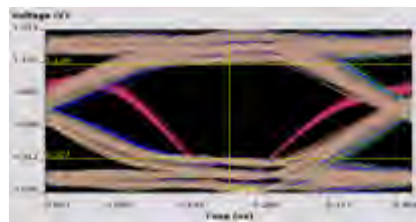
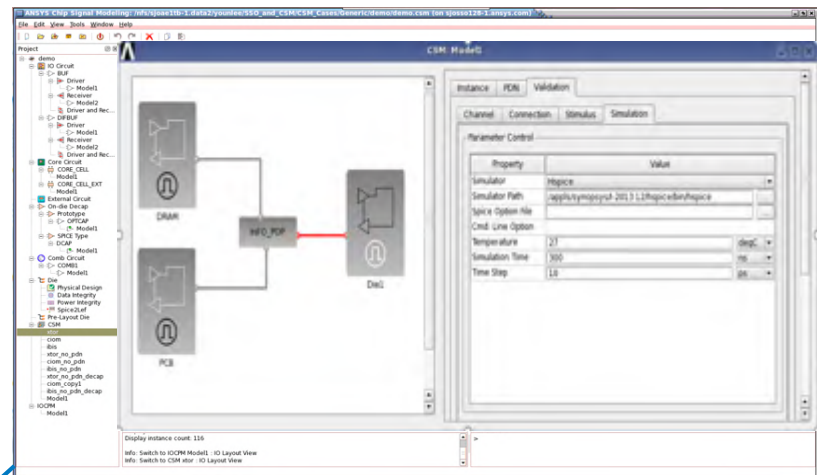
RLCG/
S-parameter



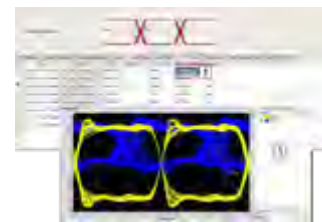
- IBIS/Xtor/CIOM
- On-chip PDN
- Intrinsic Cap of IO

Chip Model Creation for Signal Integrity

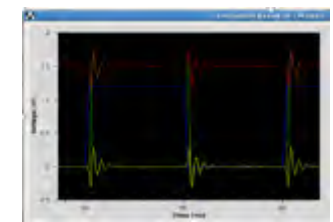
Ansyp Chip Signal Modeling



Jitter Analysis



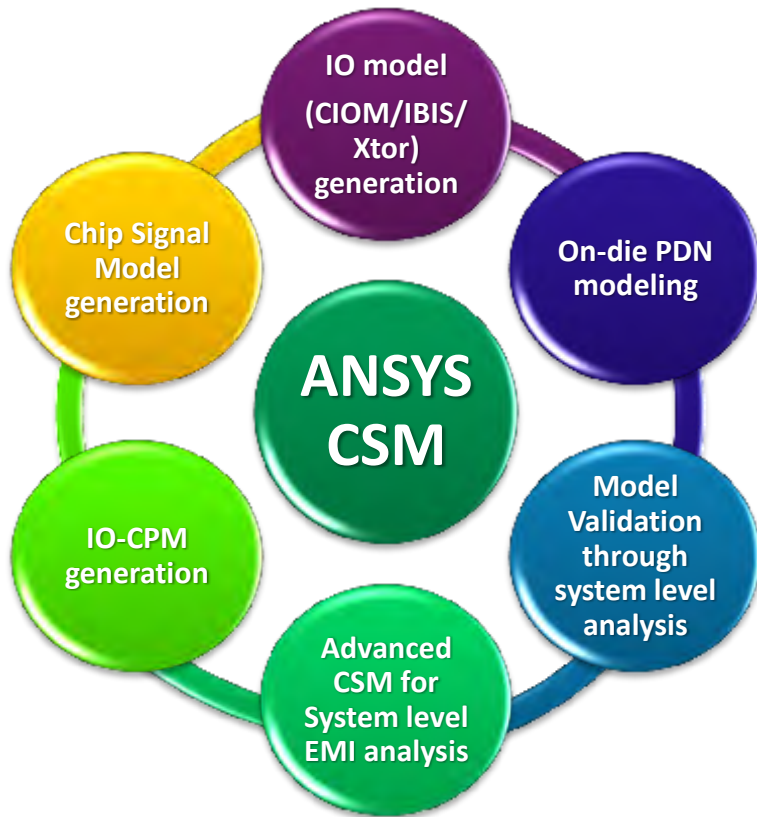
JEDEC Timing Analysis



PG Noise Analysis

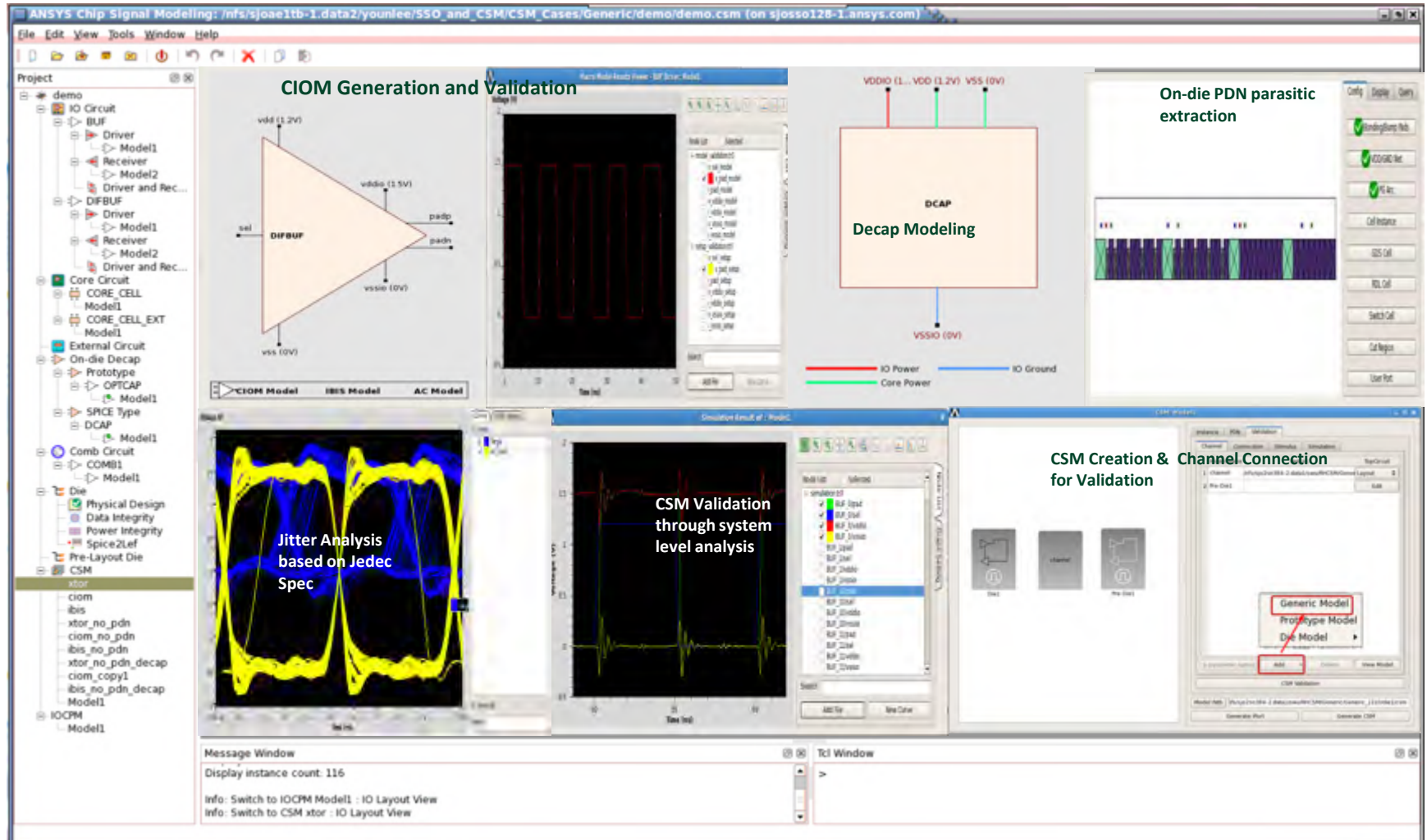
Demo Video: Extract Parasitic of Board PDN via SIwave-CPA

ANSYS Chip Signal Modeling



- Chip Model generation for DDR timing and EMI
- Chip & System level signal Integrity simulation
- Target User: Package designer, Chip DDRPHY or IO designer
- Validation includes JEDEC compatible timing, noise, jitter, slew reporting covering single ended and differential type IOs
- Customized 3DIC, HBM, WLP(Wafer Level Package) target CSM generation & validation

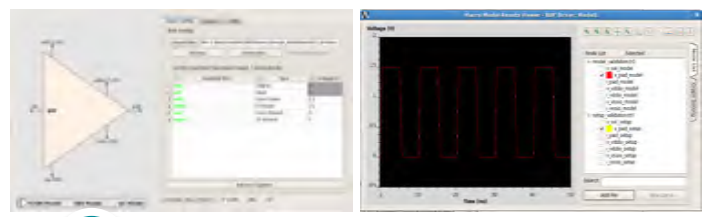
ANSYS CSM GUI Overview



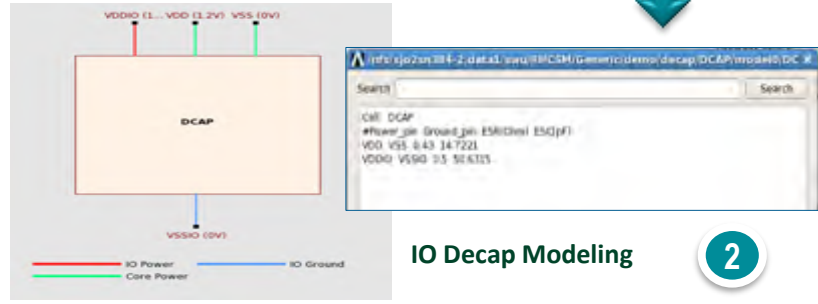
The screenshot displays the ANSYS CSM GUI interface with several key components:

- Project Tree (Left):** Lists the circuit hierarchy including IO Circuit, Core Circuit, and Die.
- CIOM Generation and Validation:** Shows a schematic of a DIFBUF component and a corresponding waveform plot.
- Decap Modeling:** Illustrates a DCAP component connected to power and ground rails (VDDIO, VDD, VSS, VSSIO).
- On-die PDN parasitic extraction:** Shows a waveform plot representing parasitic extraction results.
- Jitter Analysis based on Jeduc Spec:** Displays a complex waveform plot for jitter analysis.
- CSM Validation through system level analysis:** Shows a waveform plot for system-level validation.
- CSM Creation & Channel Connection for Validation:** Shows the configuration of CSM models (Generic Model, Prototype Model, Die Model) and their connections.
- Message Window (Bottom Left):** Displays system information such as "Display instance count: 116".

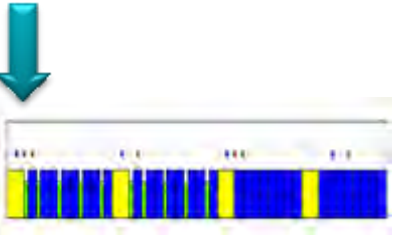
Chip Signal Model Creation and Validation Flow



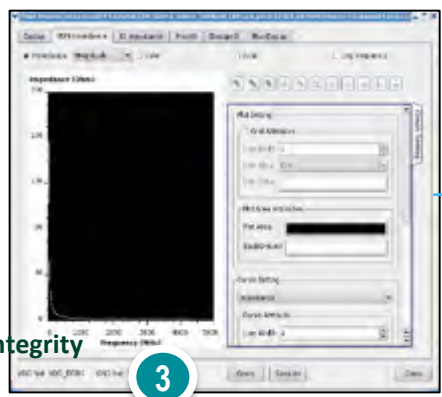
1 CIOM Generation and Validation



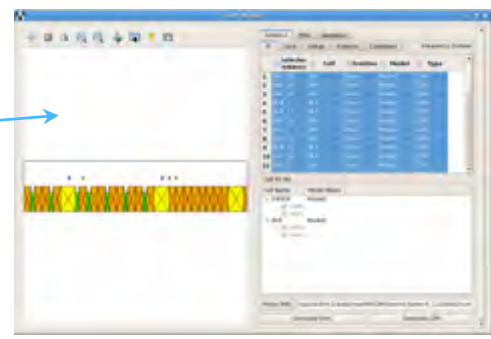
2 IO Decap Modeling



Parasitic Extraction and Power Integrity Analysis of on-chip PDN



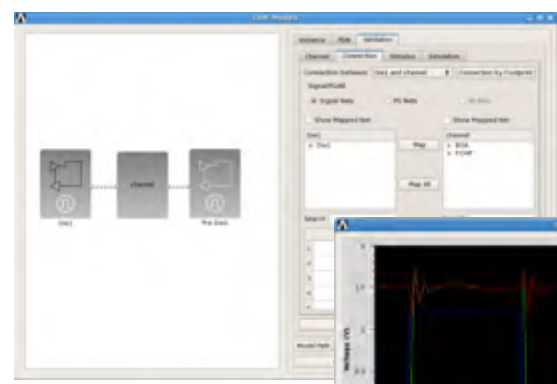
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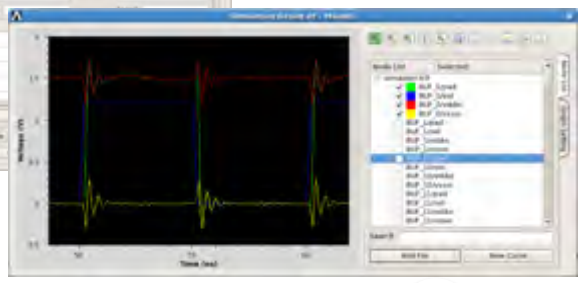
CSM(Chip Signal Model) Creation



4

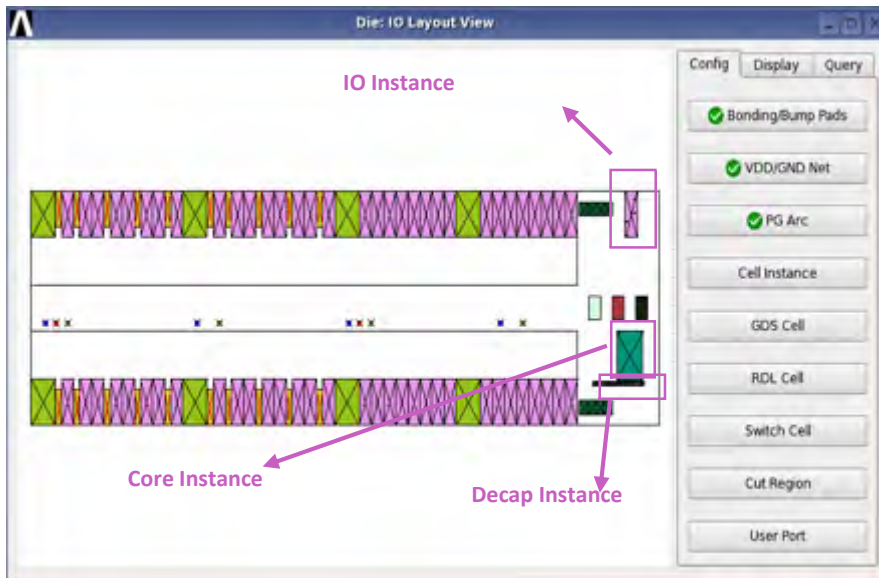


Simulation env. set up for CSM validation

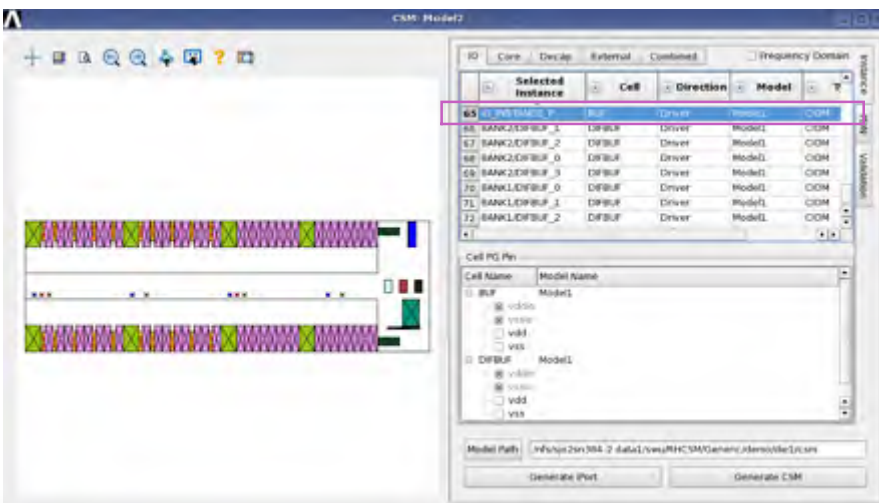


5

What-if analysis for DDRPHY IO/Decap Optimization



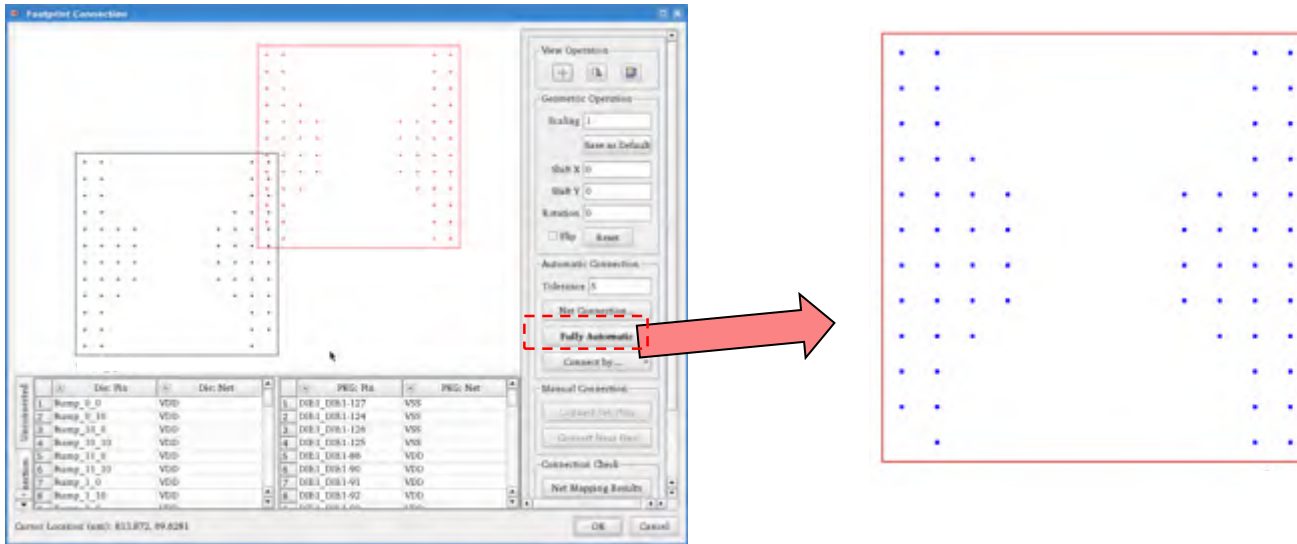
- IO/Decap/Core Instance can be newly defined or added;
- User-defined cell instances are placed in DDRPHY.



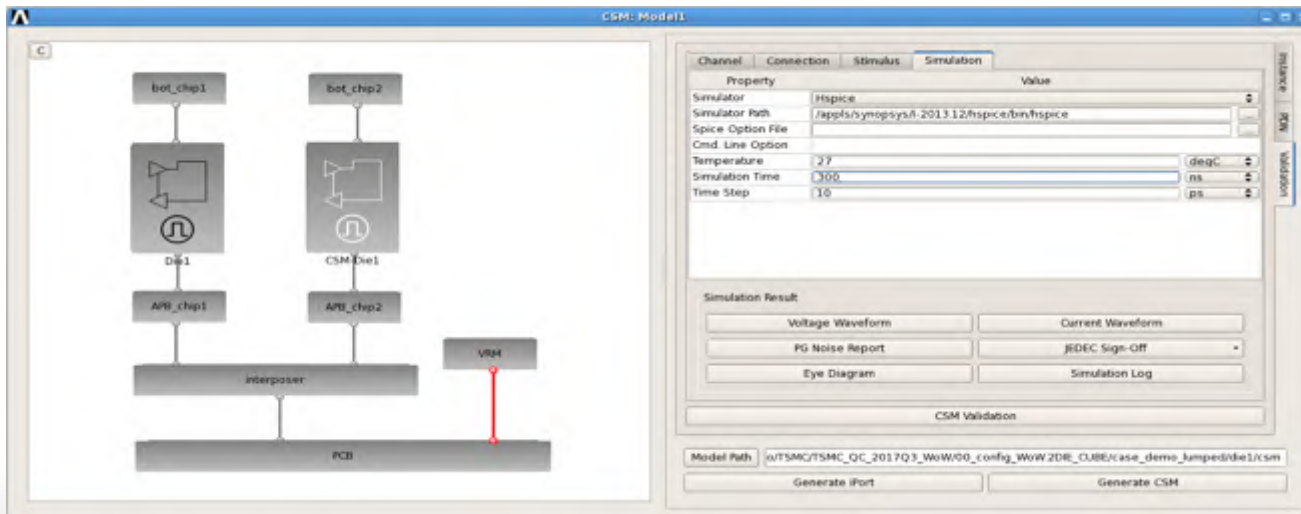
- Enables to generate various types of CSM with different optimization case;
- User can do performance check through channel simulation and select the best case.

Demon Video: CSM Model Creation of DDR Design

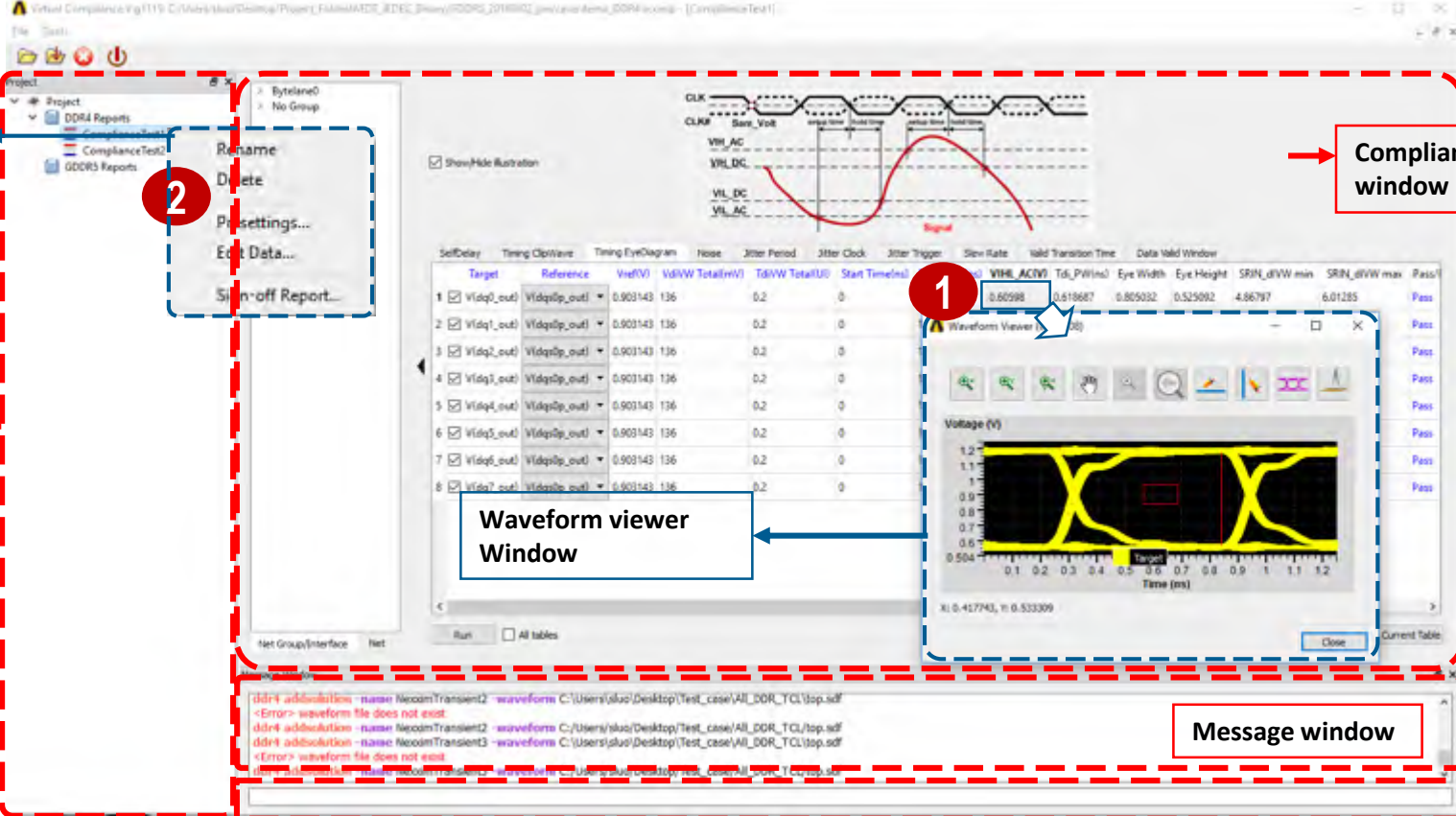
Channel Connection & Auto Simulation Test bench Creation



CSM and all parasitic models from SIwave enables auto electrical connection between driver dies, Package and Board to receiver through CPP(Chip Package Protocol) header



New Virtual Compliance GUI Overview



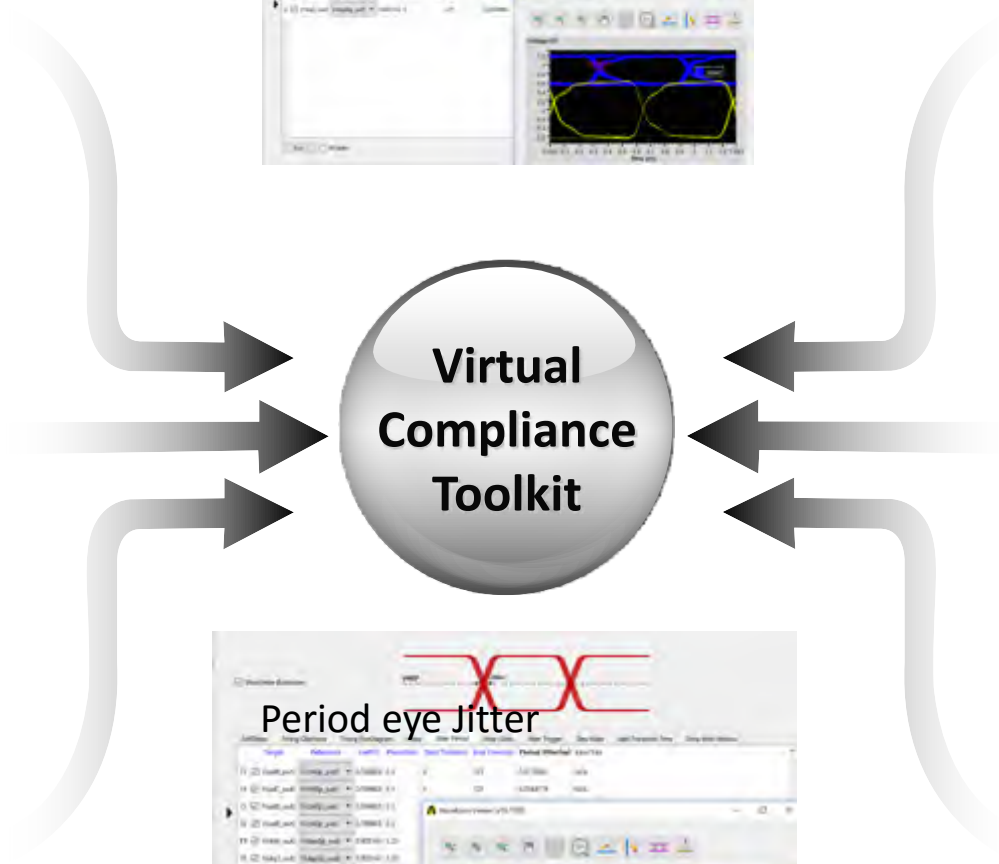
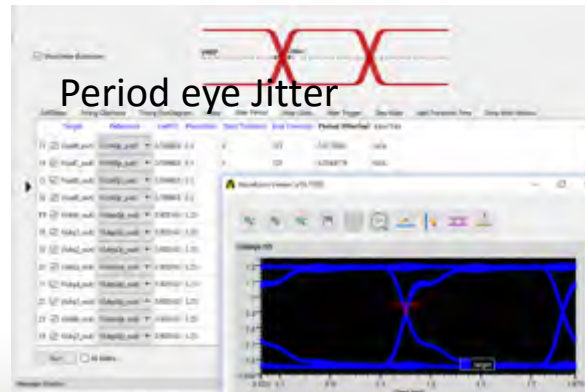
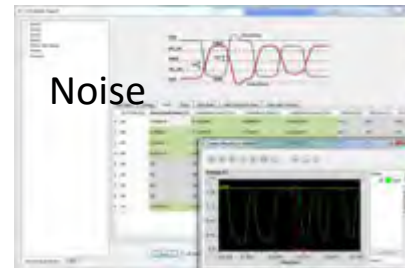
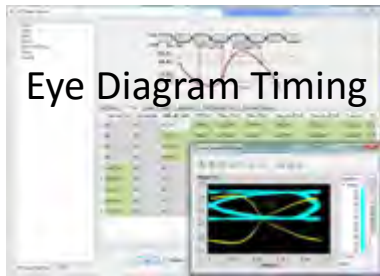
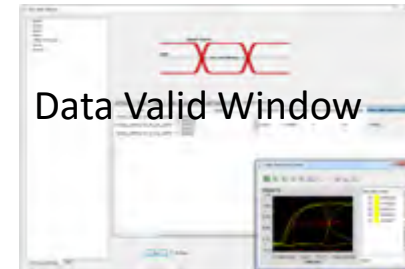
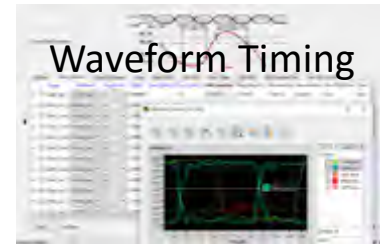
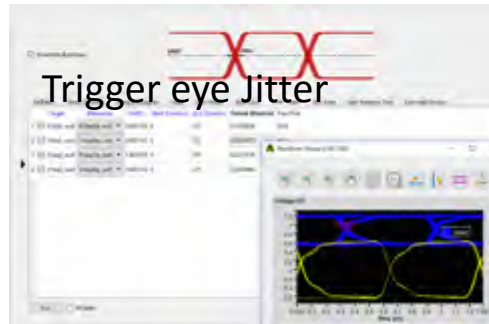
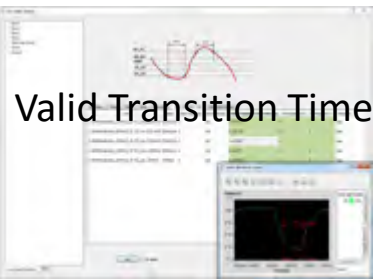
The screenshot shows the Virtual Compliance GUI interface. A red dashed box highlights the main workspace. Callouts point to various elements:

- Right click menu:** A context menu is open over the 'Compliance Test' folder in the project tree, showing options like 'Rename', 'Delete', 'Print Settings...', 'Edit Data...', and 'Sign-off Report...'. A red circle with the number '2' is next to it.
- Compliance test window:** Points to the top section of the GUI showing signal waveforms for CLK, VMH_AC, VMH_DC, VIL_DC, and VIL_AC.
- Report list window:** Points to a table listing compliance test results. A red circle with the number '1' is next to it.
- Waveform viewer Window:** A pop-up window showing a detailed waveform plot of Voltage (V) vs Time (ms).
- Message window:** A window at the bottom showing error messages: 'Error: waveform file does not exist'.
- TCL command window:** A window at the bottom right showing TCL commands and their outputs.

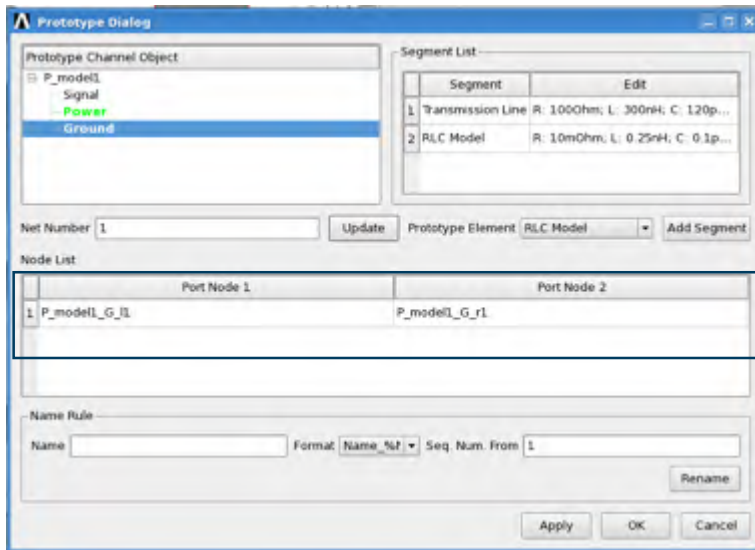
Target	Reference	Vref(V)	VdVW Total(W)	TdVW Total(U)	Start Time(s)	Pass/Fail	
1	Vldq1_out	Vldq1p_out	0.903143	136	0.2	0	Pass
2	Vldq1_out	Vldq1p_out	0.903143	136	0.2	0	Pass
3	Vldq2_out	Vldq2p_out	0.903143	136	0.2	0	Pass
4	Vldq2_out	Vldq2p_out	0.903143	136	0.2	0	Pass
5	Vldq4_out	Vldq4p_out	0.903143	136	0.2	0	Pass
6	Vldq4_out	Vldq4p_out	0.903143	136	0.2	0	Pass
7	Vldq6_out	Vldq6p_out	0.903143	136	0.2	0	Pass
8	Vldq6_out	Vldq6p_out	0.903143	136	0.2	0	Pass

1. Each report cell can pop-up a waveform viewer window
2. Right click menu can export HTML format report.

Reporting Tables Overview



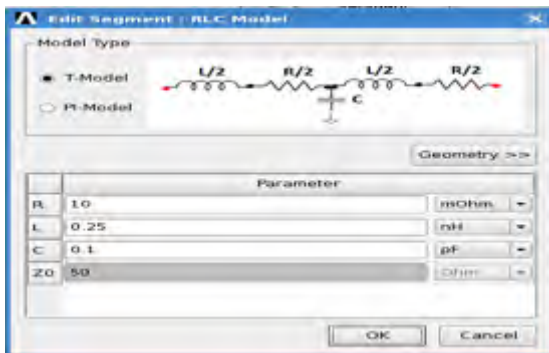
Prototype Package & Board Channel Model



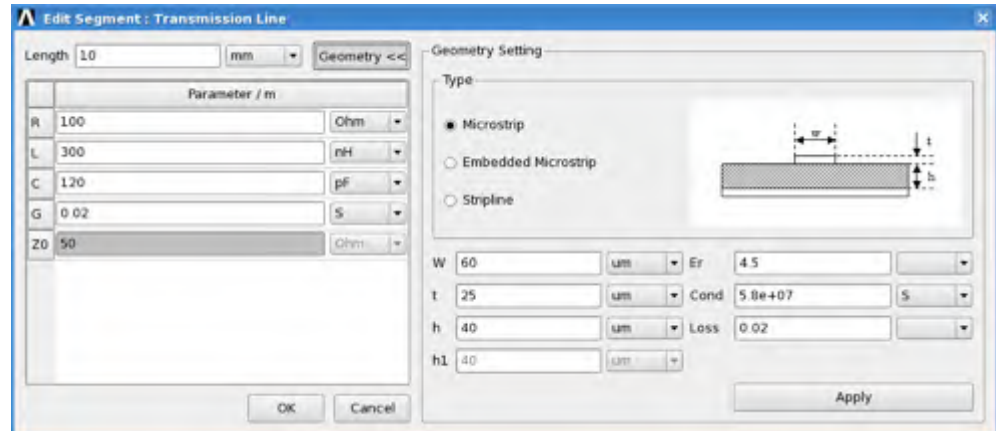
- Enables to predict performance check at the early design stage
- Instantaneous impedance(Z_0) is auto decided by RLC in the RLC Model
- RLC & Z_0 have been generated by geometry define in the Transmission Line Model
- As for multiple channel, mutual coupling effects can be defined between channels



RLC Model



Transmission Line



Demonstration Video

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感谢聆听



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