

ANSYS



仿真
新时代

2017 ANSYS用户技术大会

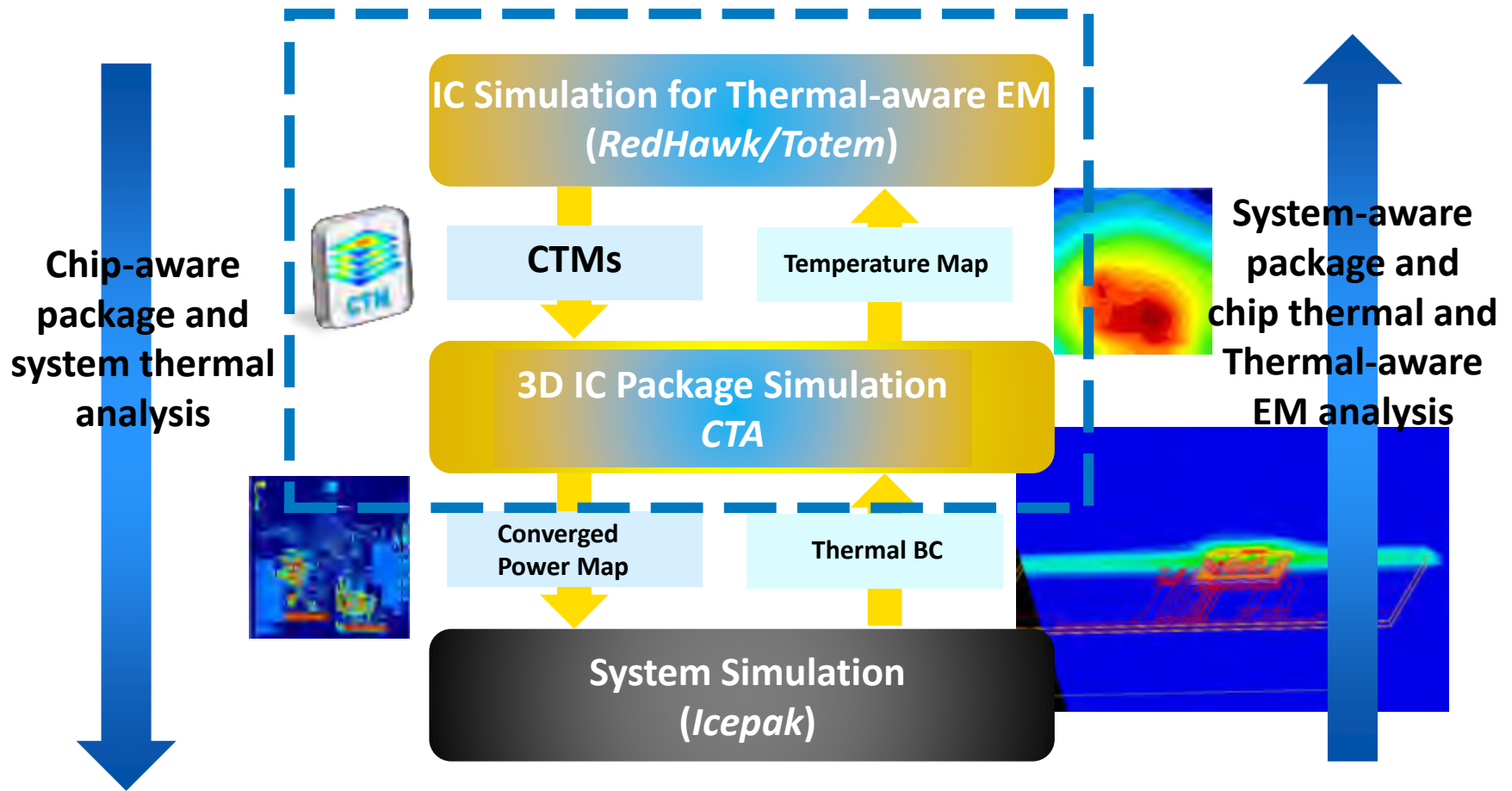
中国·烟台

Chip Package System (CPS) Thermal Integrity Co-Analysis

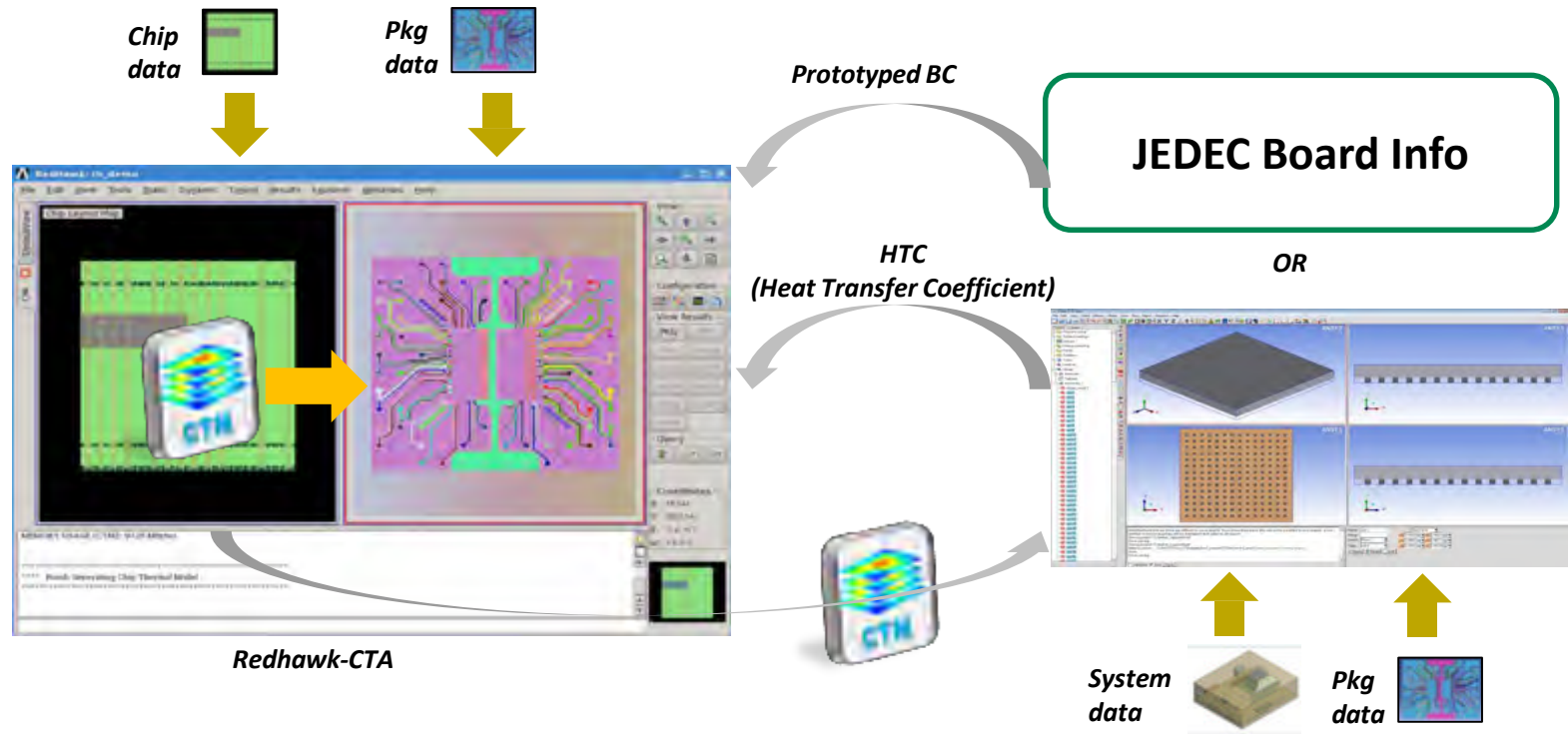
尹国丽/ Principal Product Specialist

Ansys

Chip-Package-System Thermal Integrity Solution



Chip & Board Aware Package Level Thermal Analysis



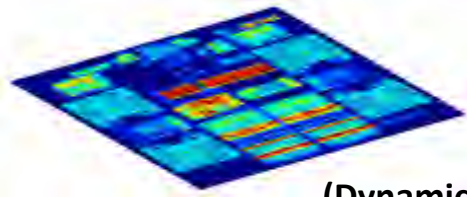
- JEDEC board is widely used for easy package level analysis when info about system is not ready or explicit

Chip Thermal Model (CTM) from RH/Totem

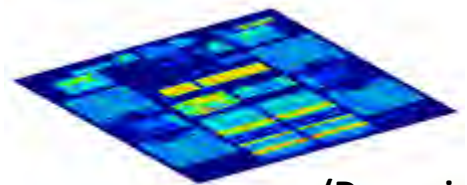
Layer stackup

Power (T)

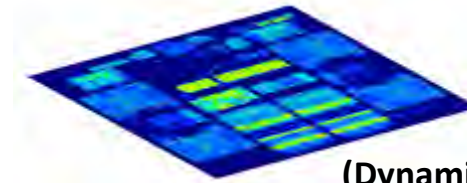
- 19: TOP_LAYER
- 18: Metal8
- 17: Via7
- 16: Metal7
- 15: Via6
- 14: Metal6
- 13: Via5
- 12: Metal5
- 11: Via4
- 10: Metal4
- 9: Via3
- 8: Metal3
- 7: Via2
- 6: Metal2
- 5: Via1
- 4: Metal1
- 3: device_2
- 2: device_1
- 1: Substrate



(Dynamic+Leakage) @T3



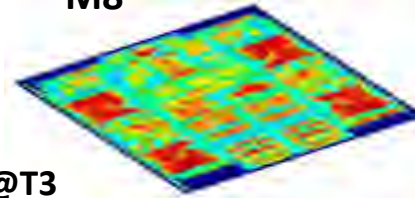
(Dynamic+Leakage) @T2



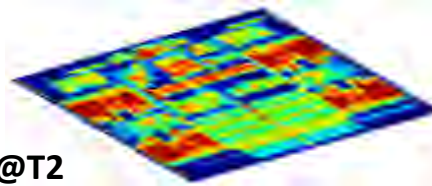
(Dynamic+Leakage) @T1

Metal Distribution

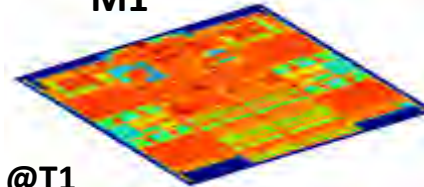
M8



M5



M1



CTM content

- Temp-dependent tile-based power density maps
- Per layer metal density map
- Block Power File (separate input)
 - OD and power info

Configuration File(GSR) Setting for Thermal Analysis

- **Specify Package Design and Result Directory**

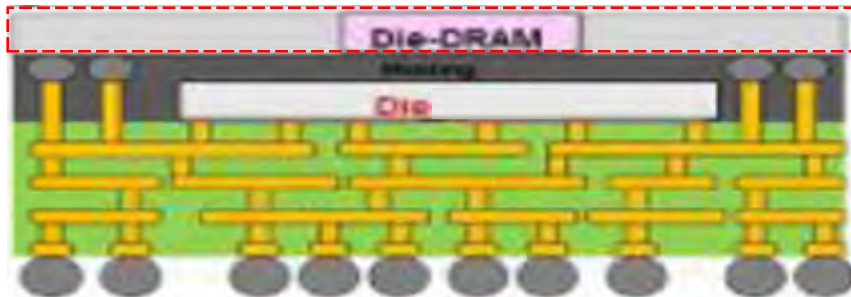
```
CPA_FILES {  
  PACKAGE          ./design.mcm  
  MODEL            ./adsCTA  
}
```

- **Must-have Option**

```
THERMAL_ANALYSIS 1
```

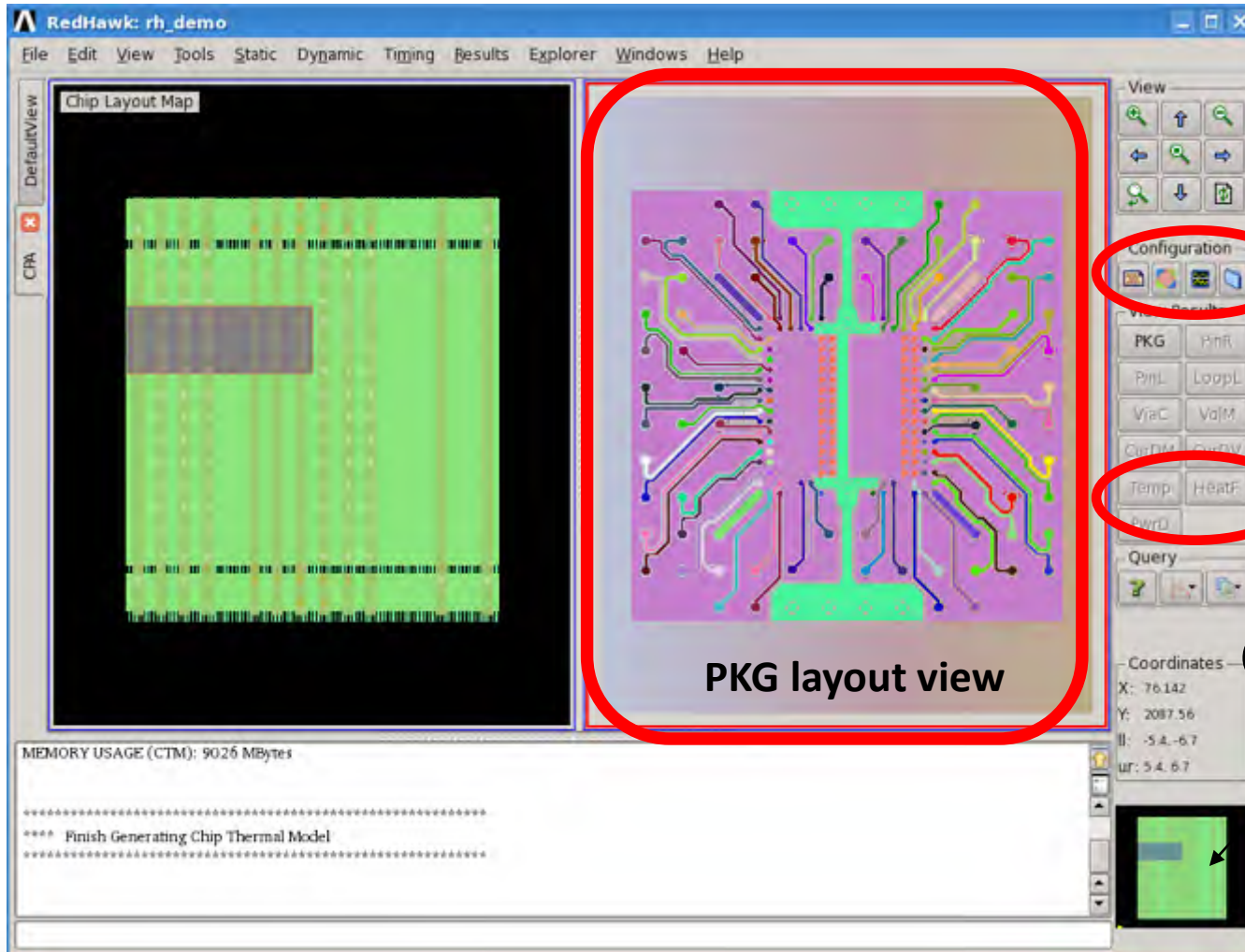
Test Design Example: POP Design

50 C



- DRAM + Die + Interposer/Package + Thermal Board
- Prescribed temperature of 50C on DRAM
- CTM power maps on Die (from RH)

Invoke RedHawk/Totem-CTA

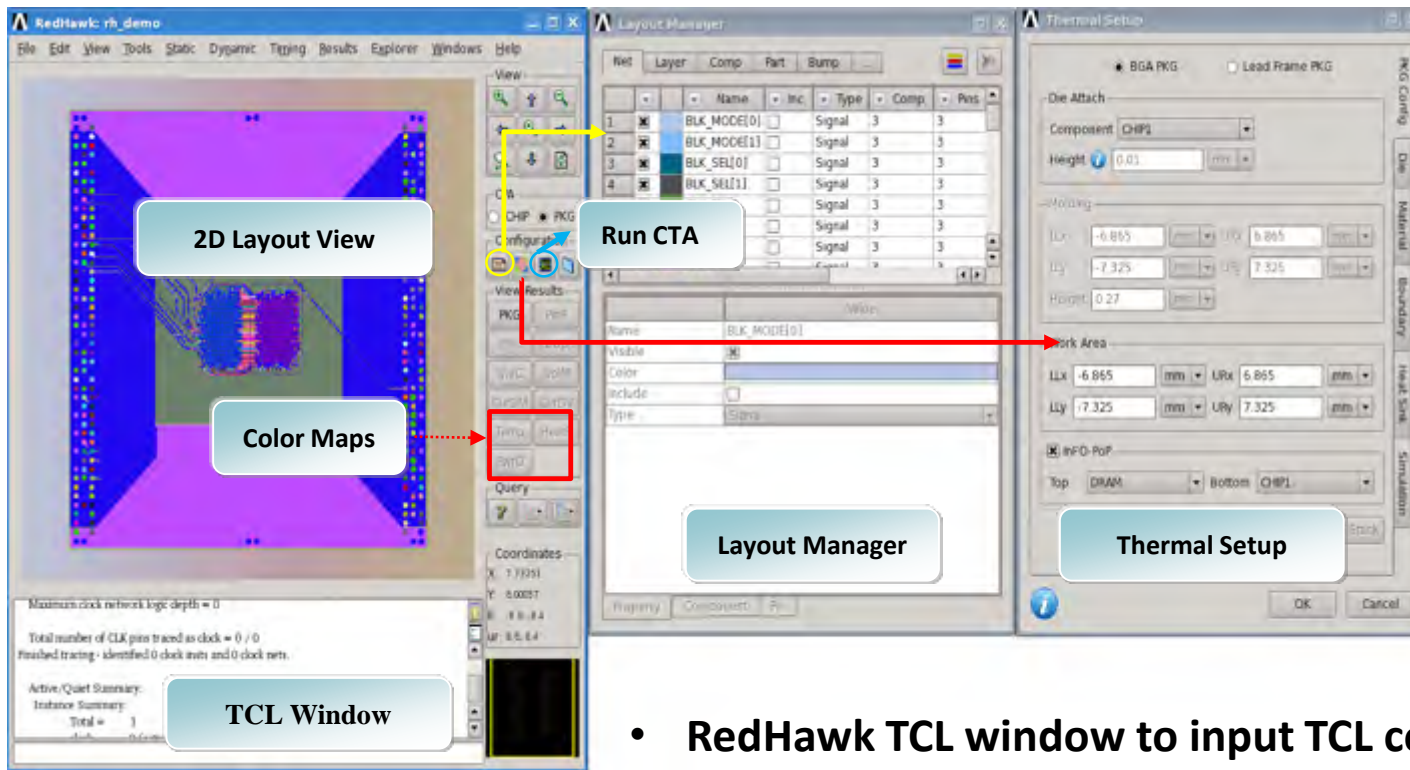


**Geometry
UI Setup**

Color maps

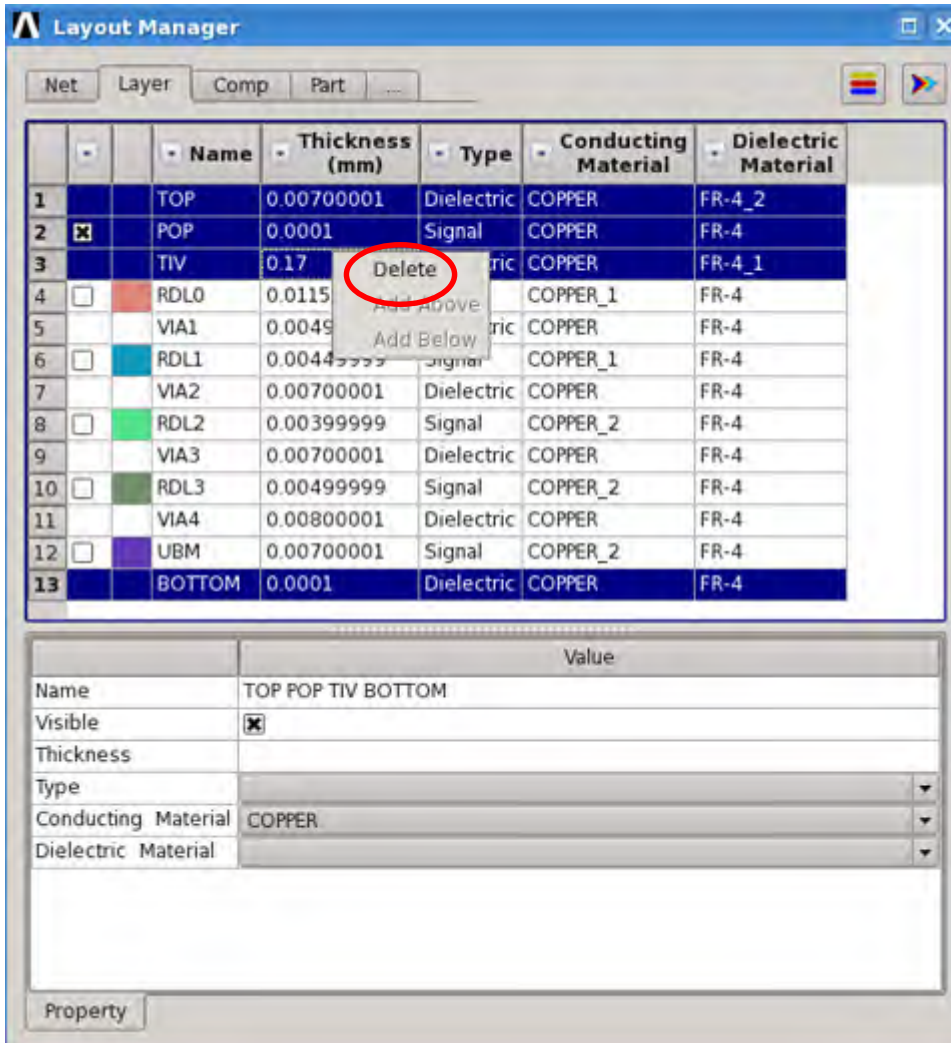
Chip Layout

Key Functions for Thermal Analysis



- RedHawk TCL window to input TCL commands
- Layout Manager for layout editing
- Thermal Setup dialog for all CTA setup
- Color Contours to Display Results

Design Setup through Layout Manager



The screenshot shows the 'Layout Manager' window with a table of layer properties. The 'TIV' layer (row 3) is selected, and a context menu is open over it, with the 'Delete' option circled in red. Below the table is a 'Property' section with fields for Name, Visible, Thickness, Type, Conducting Material, and Dielectric Material.

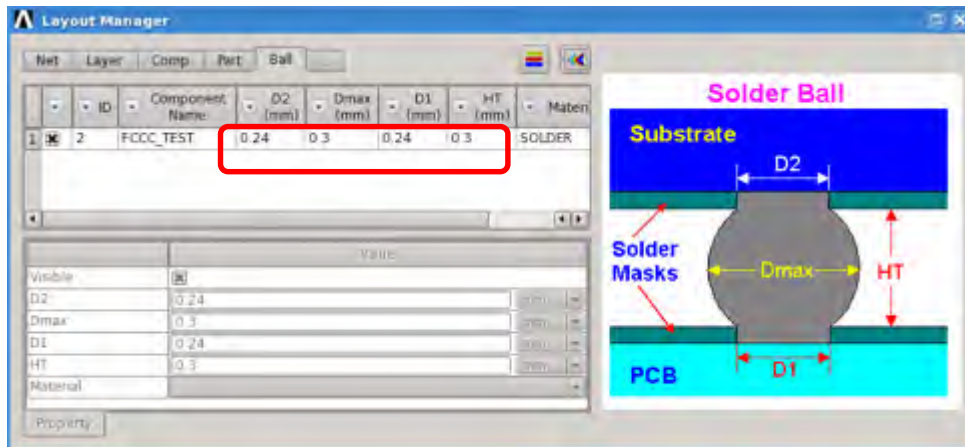
	Name	Thickness (mm)	Type	Conducting Material	Dielectric Material
1	TOP	0.00700001	Dielectric	COPPER	FR-4_2
2	POP	0.0001	Signal	COPPER	FR-4
3	TIV	0.17	Dielectric	COPPER	FR-4_1
4	RDL0	0.0115	Signal	COPPER_1	FR-4
5	VIA1	0.0049	Dielectric	COPPER	FR-4
6	RDL1	0.0044	Signal	COPPER_1	FR-4
7	VIA2	0.00700001	Dielectric	COPPER	FR-4
8	RDL2	0.00399999	Signal	COPPER_2	FR-4
9	VIA3	0.00700001	Dielectric	COPPER	FR-4
10	RDL3	0.00499999	Signal	COPPER_2	FR-4
11	VIA4	0.00800001	Dielectric	COPPER	FR-4
12	UBM	0.00700001	Signal	COPPER_2	FR-4
13	BOTTOM	0.0001	Dielectric	COPPER	FR-4

Property section:

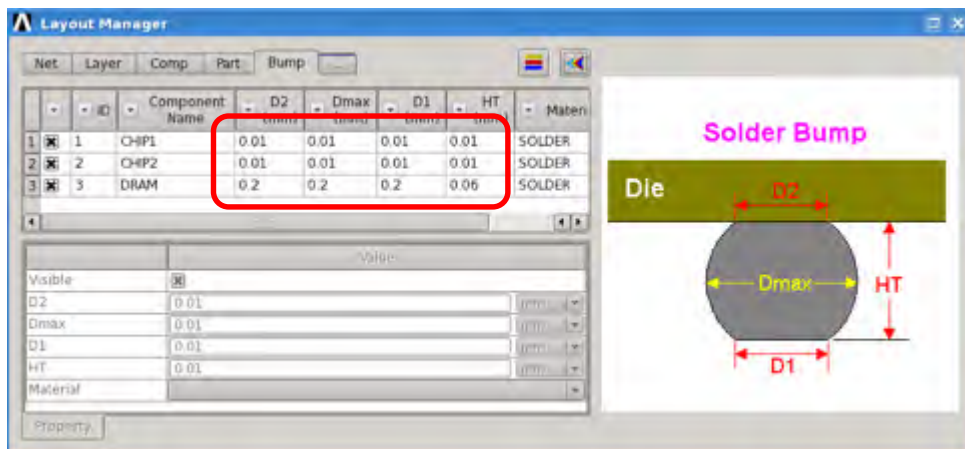
Name	TOP POP TIV BOTTOM
Visible	<input checked="" type="checkbox"/>
Thickness	
Type	
Conducting Material	COPPER
Dielectric Material	

- Set thickness, layer type
conductive/dielectric material of
target design
- Remove unnecessary layer info
- Various setting for design
optimization through what-if
analysis

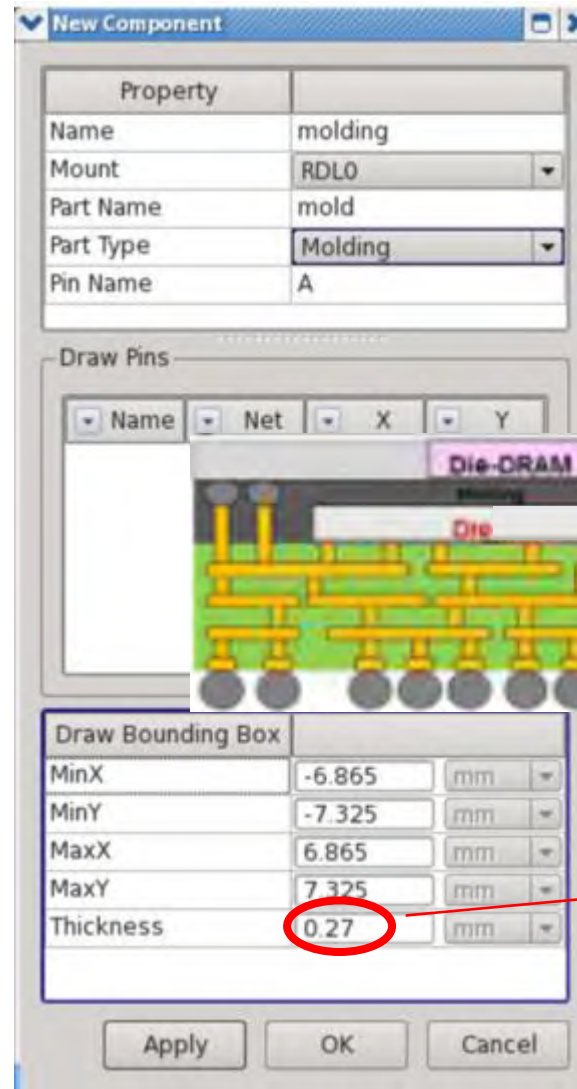
Specify Info for Bump/Ball



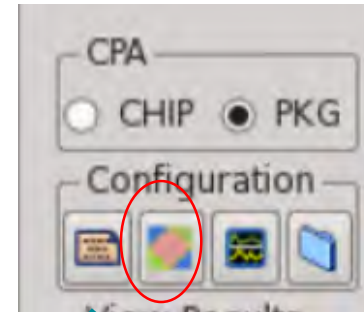
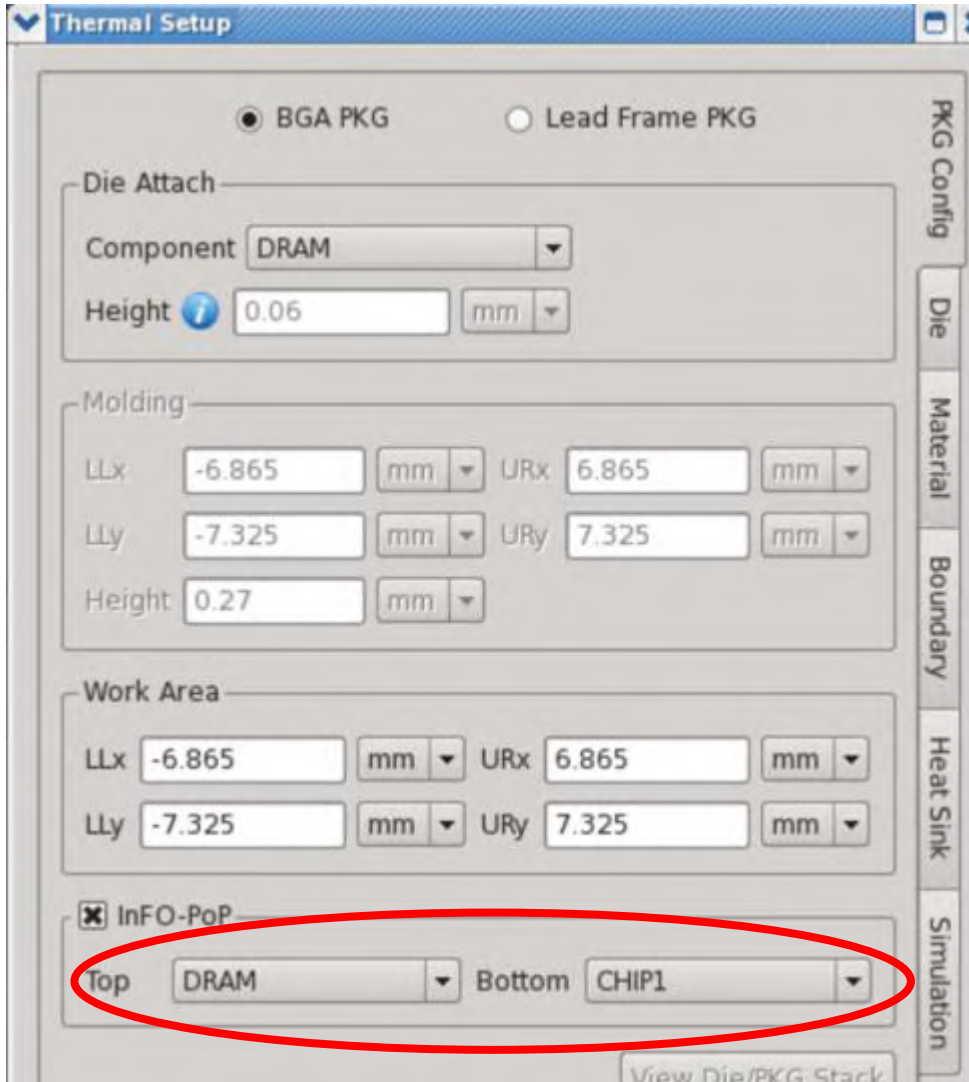
- Change Bump/Ball to practical values
- Bump/Ball are crucial info related to heat transfer



Add Molding to enclose Package and Die

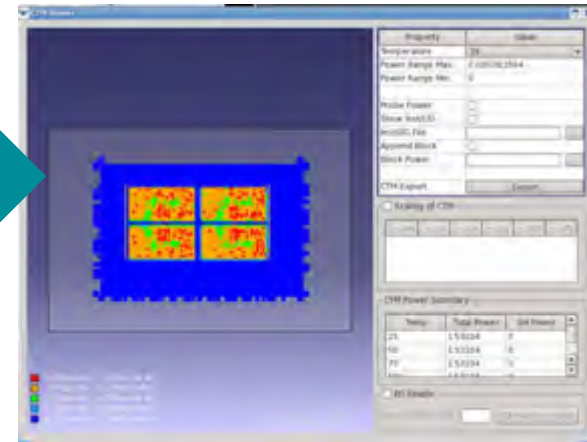
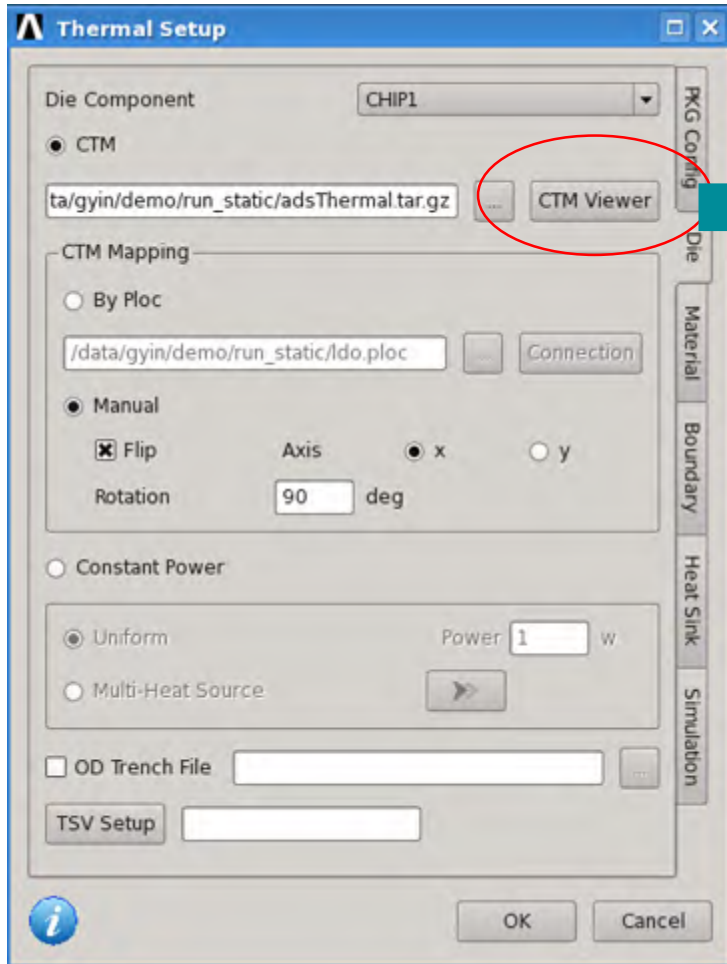


Set Up Package Configuration



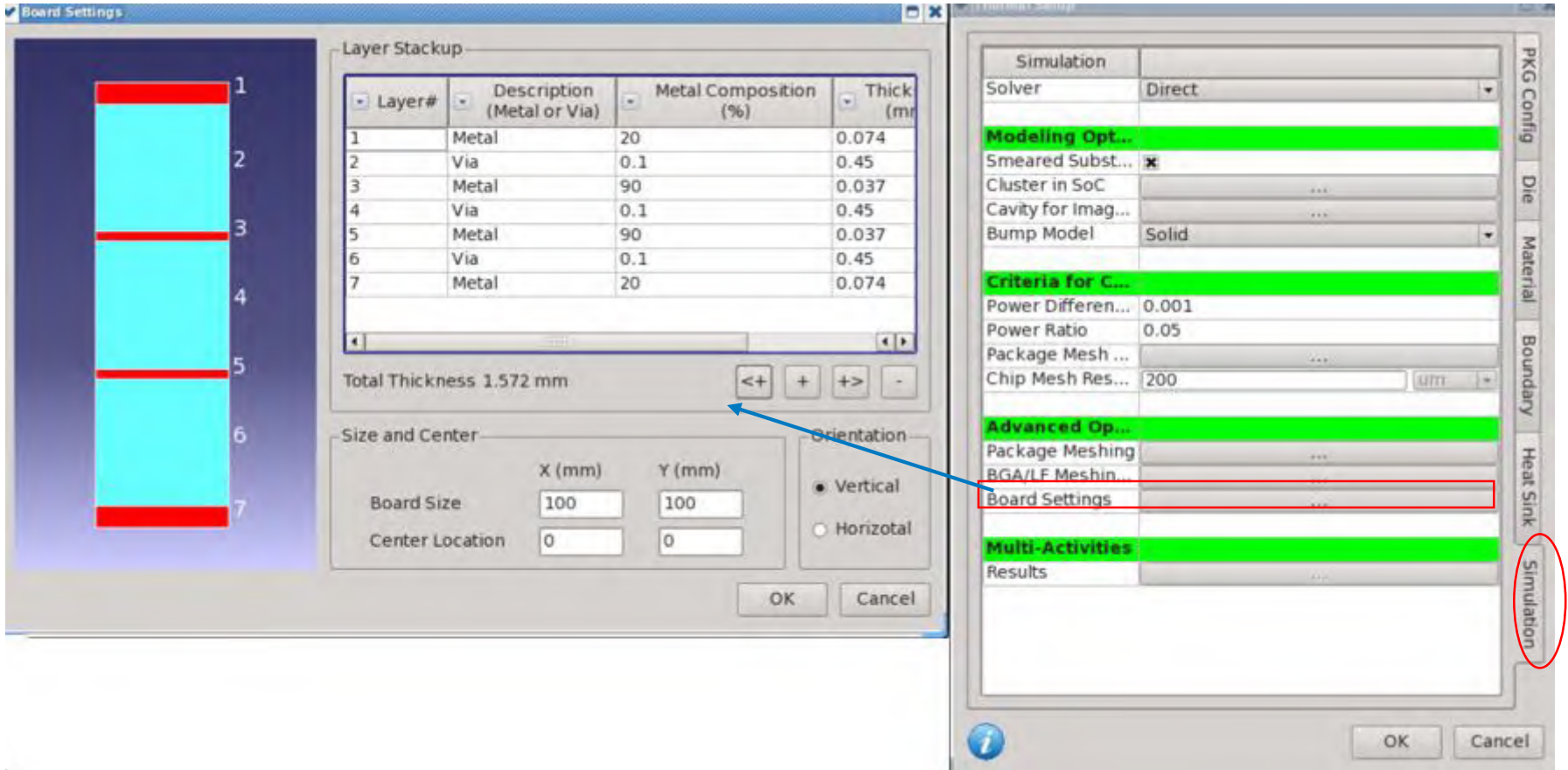
- Stackup of DRAM on Die, i.e., DRAM on top of CHIP1

Heat Source Define: CTM, OD, Power Map



- For three die components, user needs to specify its CTM model or uniform power individually.
- If die adopts CTM power model, also specify its flip/Axis/rotation values to match package design and CTM power map

JEDEC Board Setting in RH-CTA



Board Settings

Layer Stackup

Layer#	Description (Metal or Via)	Metal Composition (%)	Thick (mm)
1	Metal	20	0.074
2	Via	0.1	0.45
3	Metal	90	0.037
4	Via	0.1	0.45
5	Metal	90	0.037
6	Via	0.1	0.45
7	Metal	20	0.074

Total Thickness 1.572 mm

Size and Center

Board Size: X (mm) 100, Y (mm) 100

Center Location: X (mm) 0, Y (mm) 0

Orientation: Vertical, Horizontal

Simulation

Solver: Direct

Modeling Opt... (highlighted)

Smeared Subst...

Cluster in SoC: ...

Cavity for Imag...: ...

Bump Model: Solid

Criteria for C... (highlighted)

Power Differen...: 0.001

Power Ratio: 0.05

Package Mesh ...: ...

Chip Mesh Res...: 200

Advanced Op... (highlighted)

Package Meshing: ...

BGA/LF Meshin...: ...

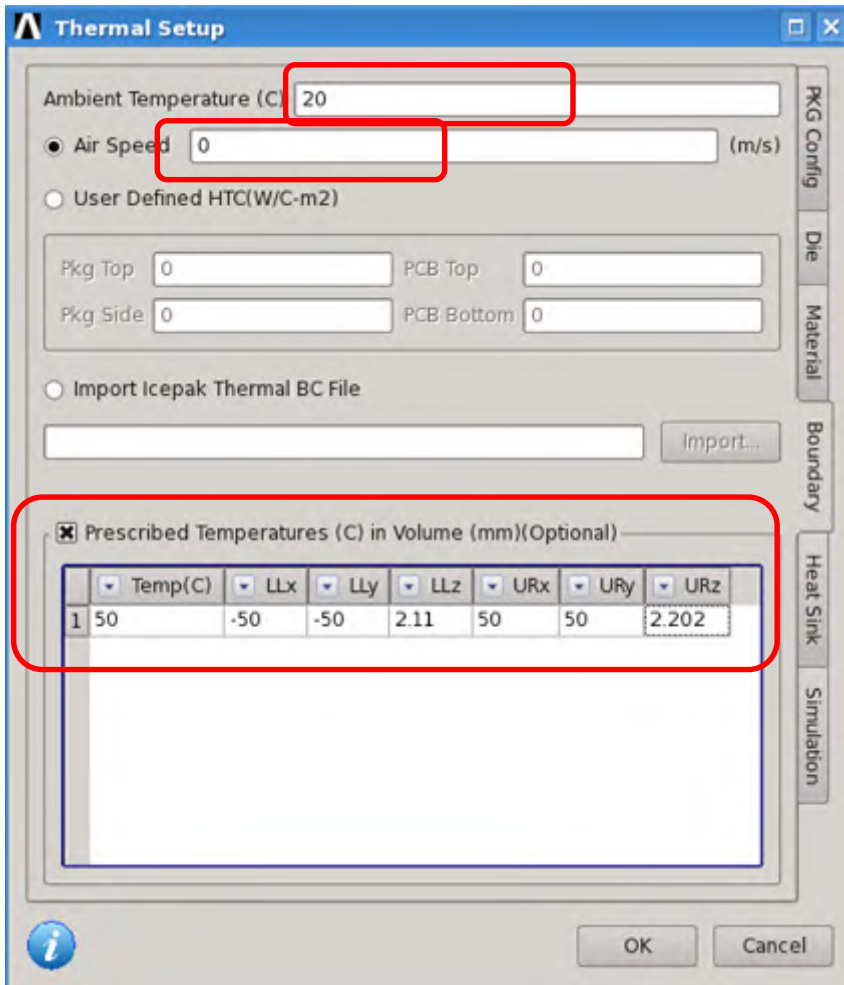
Board Settings (highlighted in red)

Multi-Activities (highlighted)

Results: ...

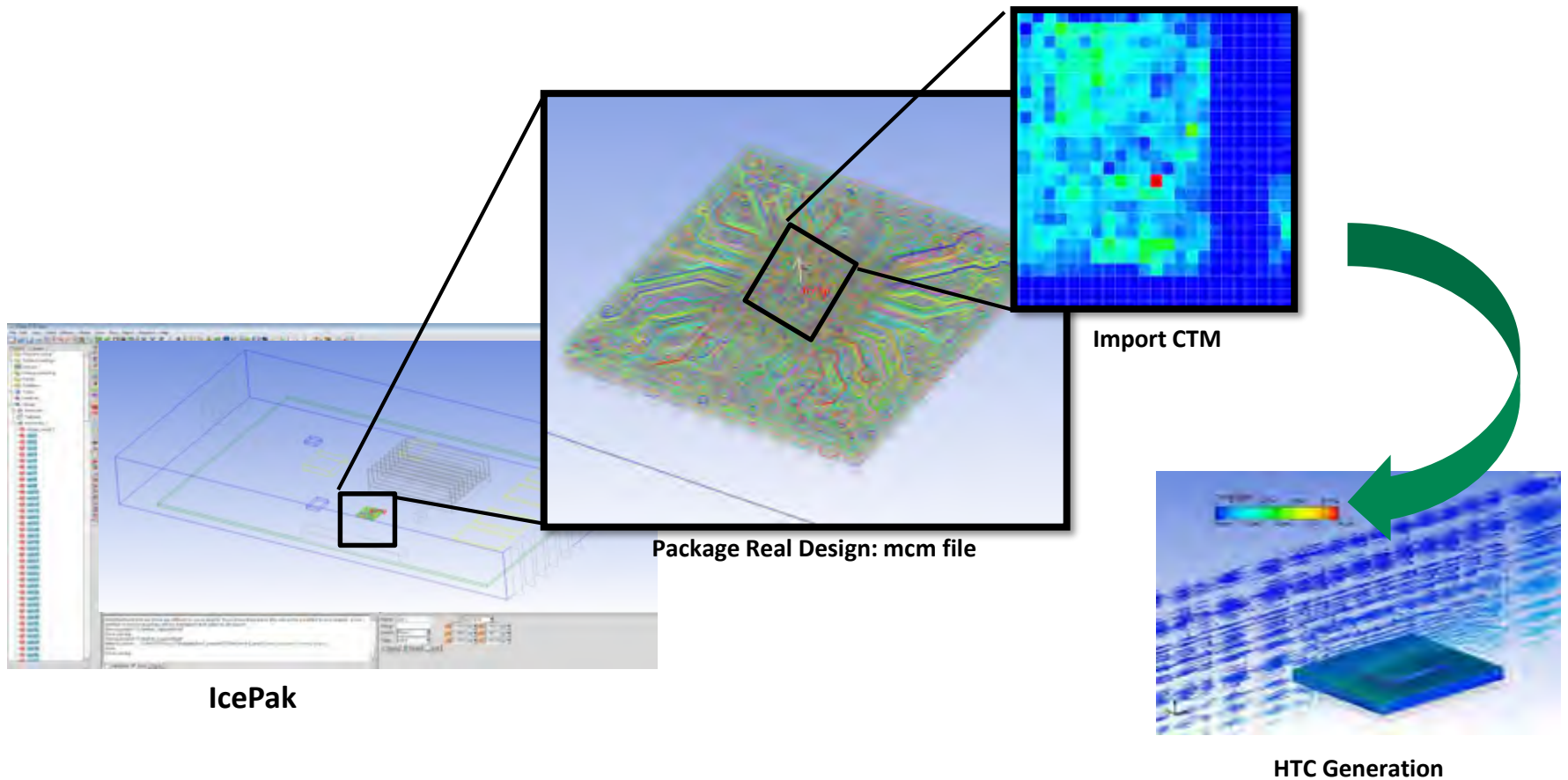
PKG Config | Die | Material | Boundary | Heat Sink | **Simulation** (circled in red)

Thermal Boundary Condition(BC) Set up

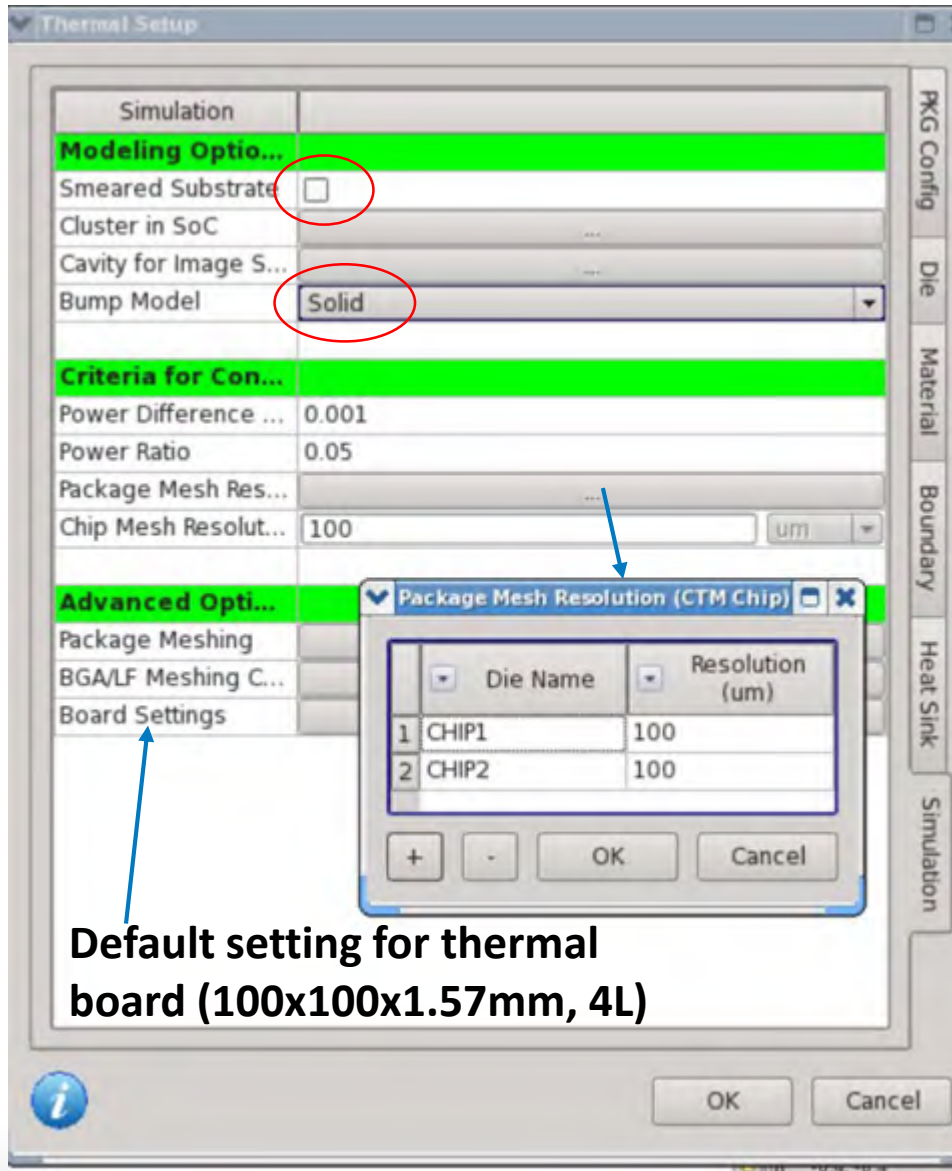


- Import HTC from IcePak or User-defined
- User-defined setup example
 - Specify env temperature; default 20C
 - Specify Air speed 0;
 - Specify prescribed temperature on top of DRAM

HTC Generation from IcePak



Simulation Configurations



All layers modeled explicitly

Solid elements for bumps/TIV

100um resolution for CTM dies

Default setting for thermal board (100x100x1.57mm, 4L)

Thermal Analysis Results

Layout Manager <@sjofoundry256-1.ansys.com>

Net Layer Comp Part Post

Post-Processing Type

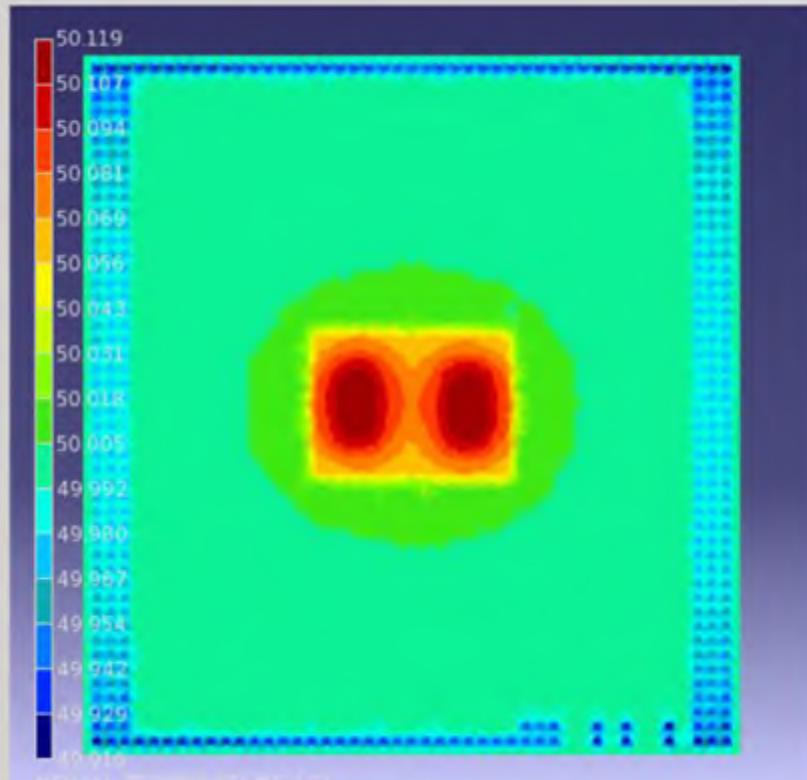
1 Thermal Analysis

	Value
Visibility	<input checked="" type="checkbox"/>
Result Type	NODAL-TEMPERATURE (C)
CHIP1 Layers	
CHIP2 Layers	
Package Layers	DA_DRAM
Board Layers	
Contour Range	Auto
Transparency	60
Flip Color Map	<input type="checkbox"/>

Property

RedHawk: rh_demo <@sjofoundry256-1.ansys.com>

File Edit View Tools Static Dynamic Timing Results Explorer Windows Help



View

CPA

CHIP PKG

Configuration

View Results

PKG PinR

PinL LoopL

ViaC VolM

CurDM CurDV

Temp HeatF

PwrD

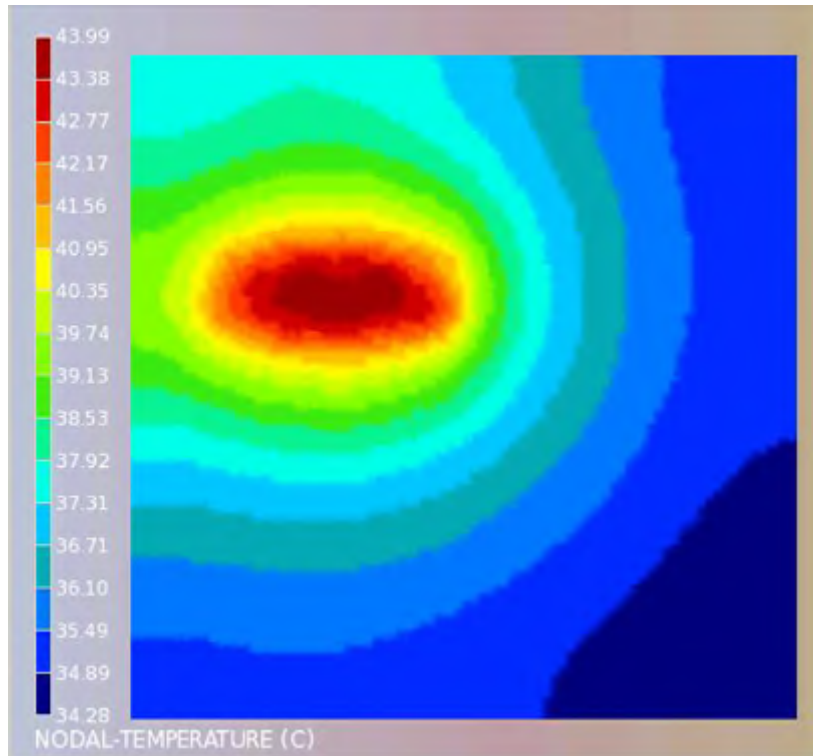
Query

Coordinates

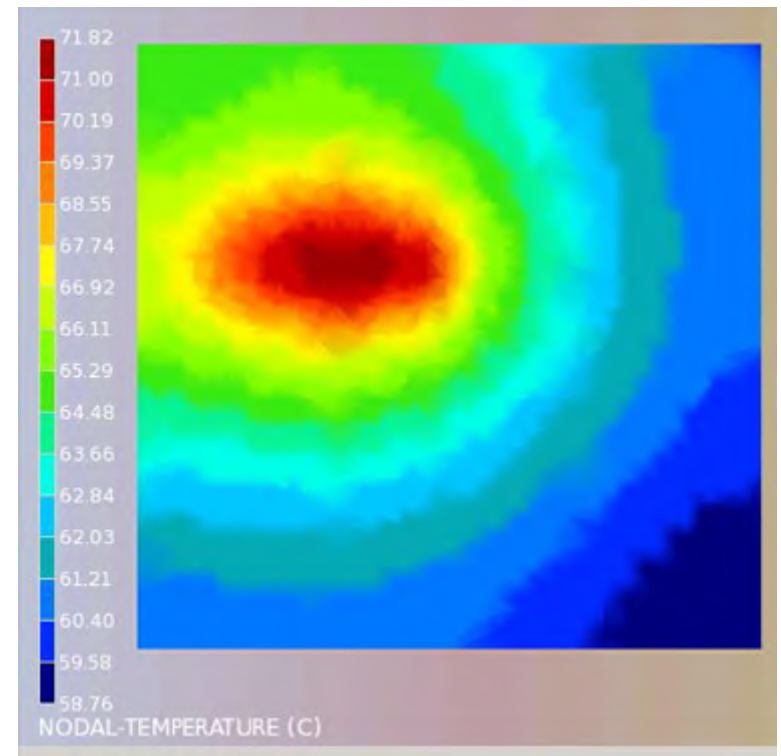
X: -7.90745

Y: -3.83127

Package Level Thermal Profile vs. Heat Source



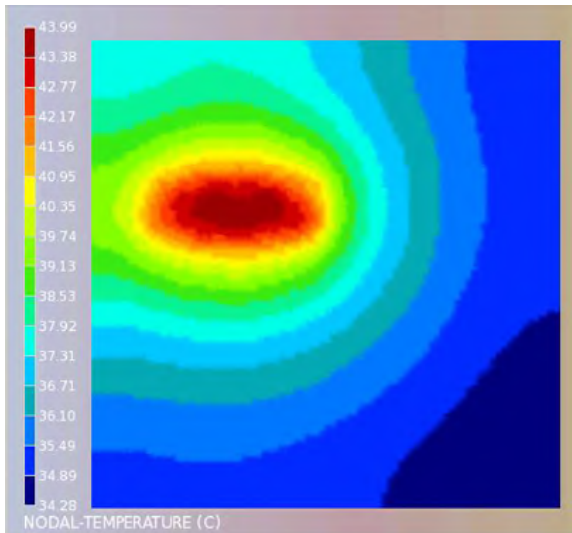
CTM(Chip Thermal Model)



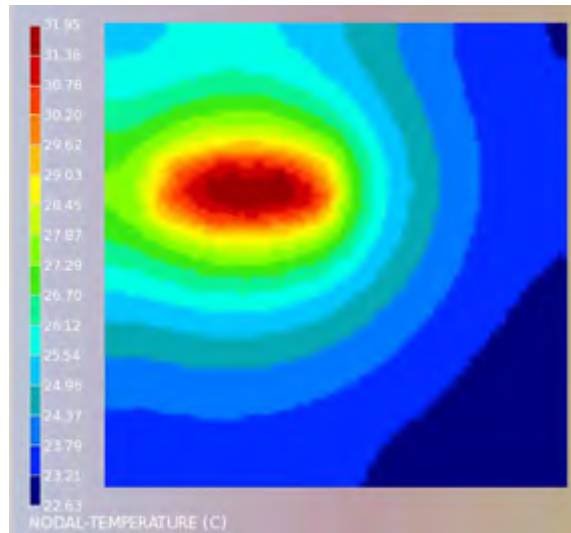
30x30 Bin-based Power Map

- Wrong power map can lead to a wrong temperature result

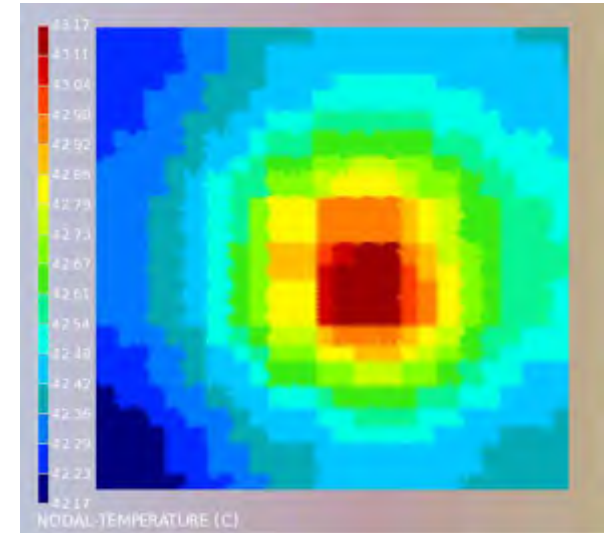
Package Level Thermal Profile vs. HTC



Without HTC



HTC based on
Prototyped BC



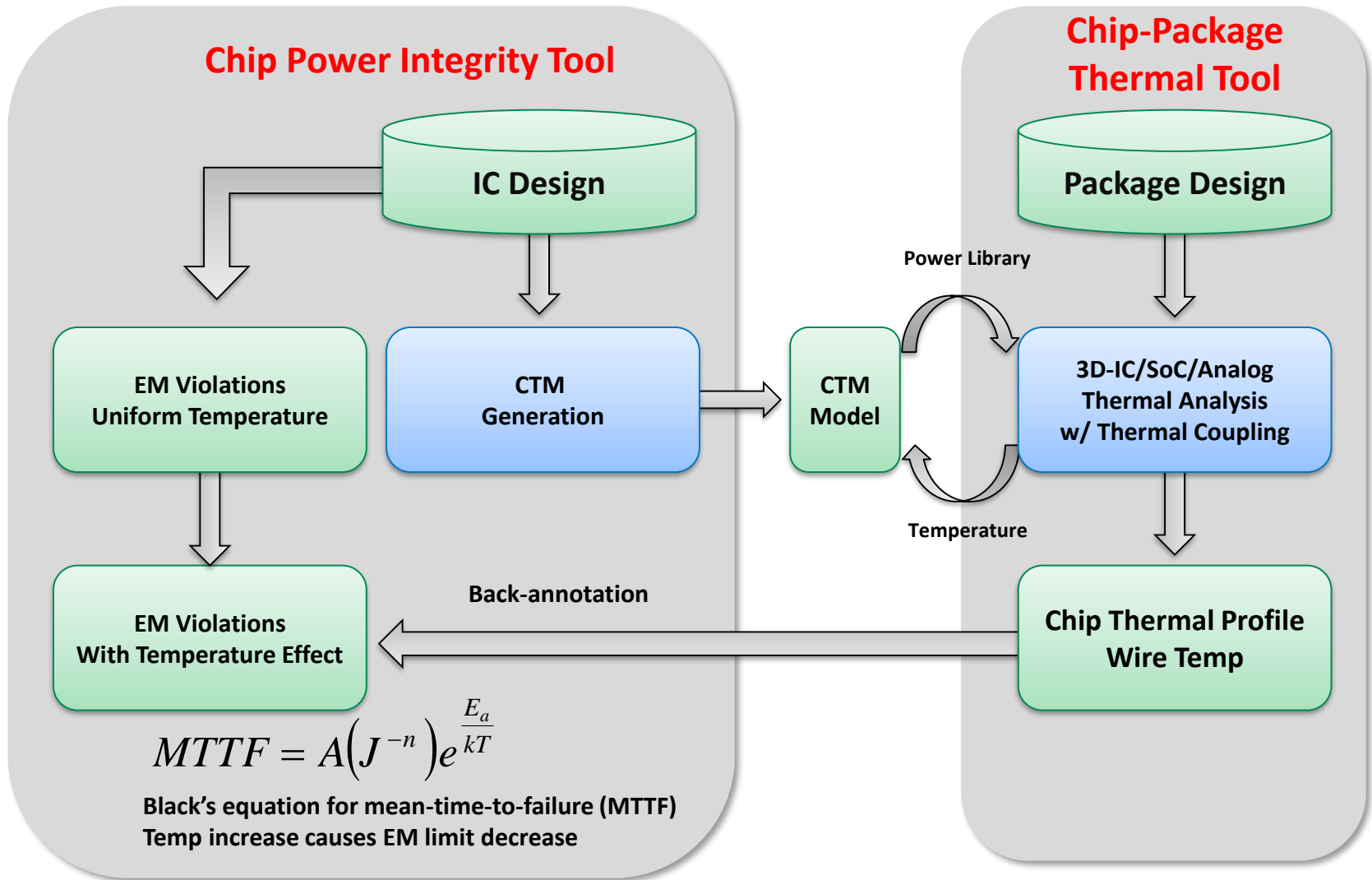
HTC from IcePak

- **Hotspot and thermal profiles are different according to boundary condition and board design info**
- **CPS integrated solution is necessary for accuracy**

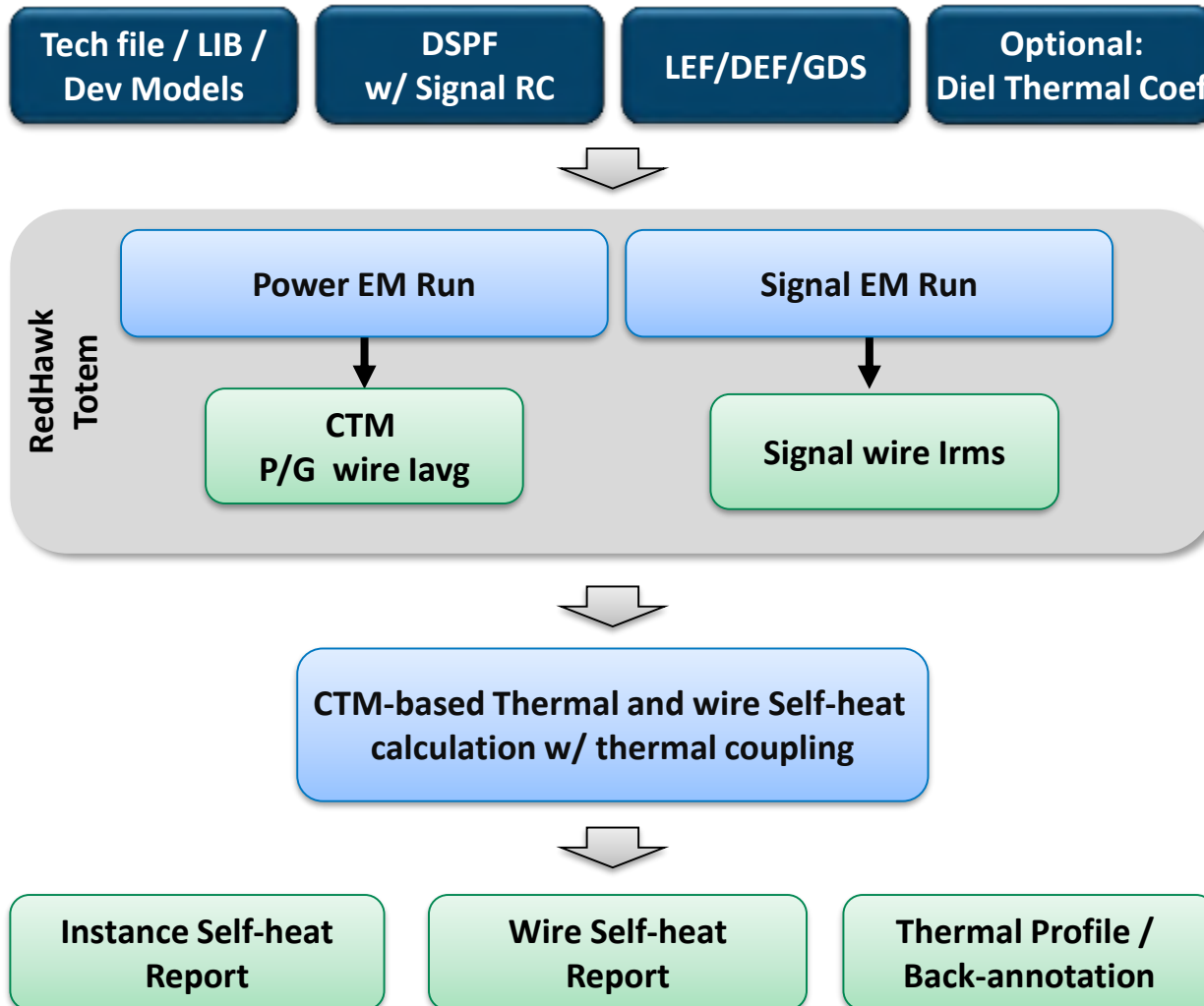
Demo Video

- **Should includes**
 - Design Set up for package level thermal analysis
 - CTM generation and import
 - Boundary condition and Jedec board setting
 - Thermal analysis and result show

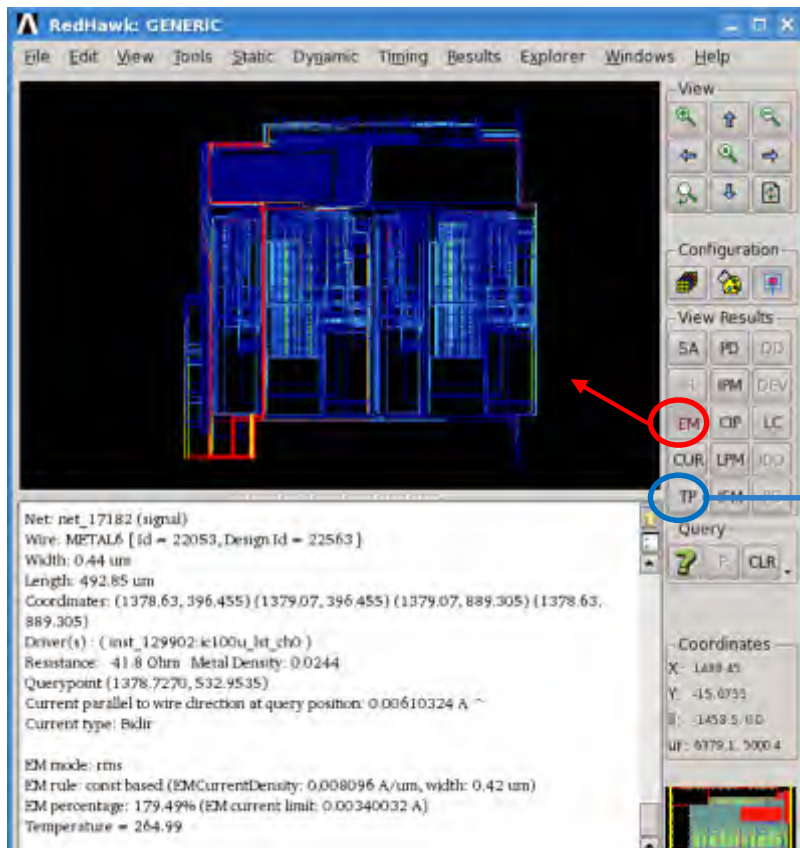
Chip-Package-System Thermal-Aware EM Flow



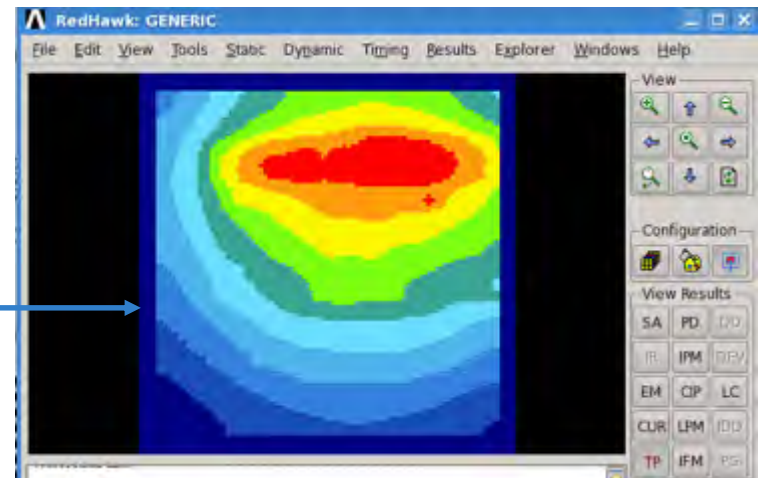
Self-heat Calculation Flow in RedHawk/Totem



RedHawk – View Thermal Maps



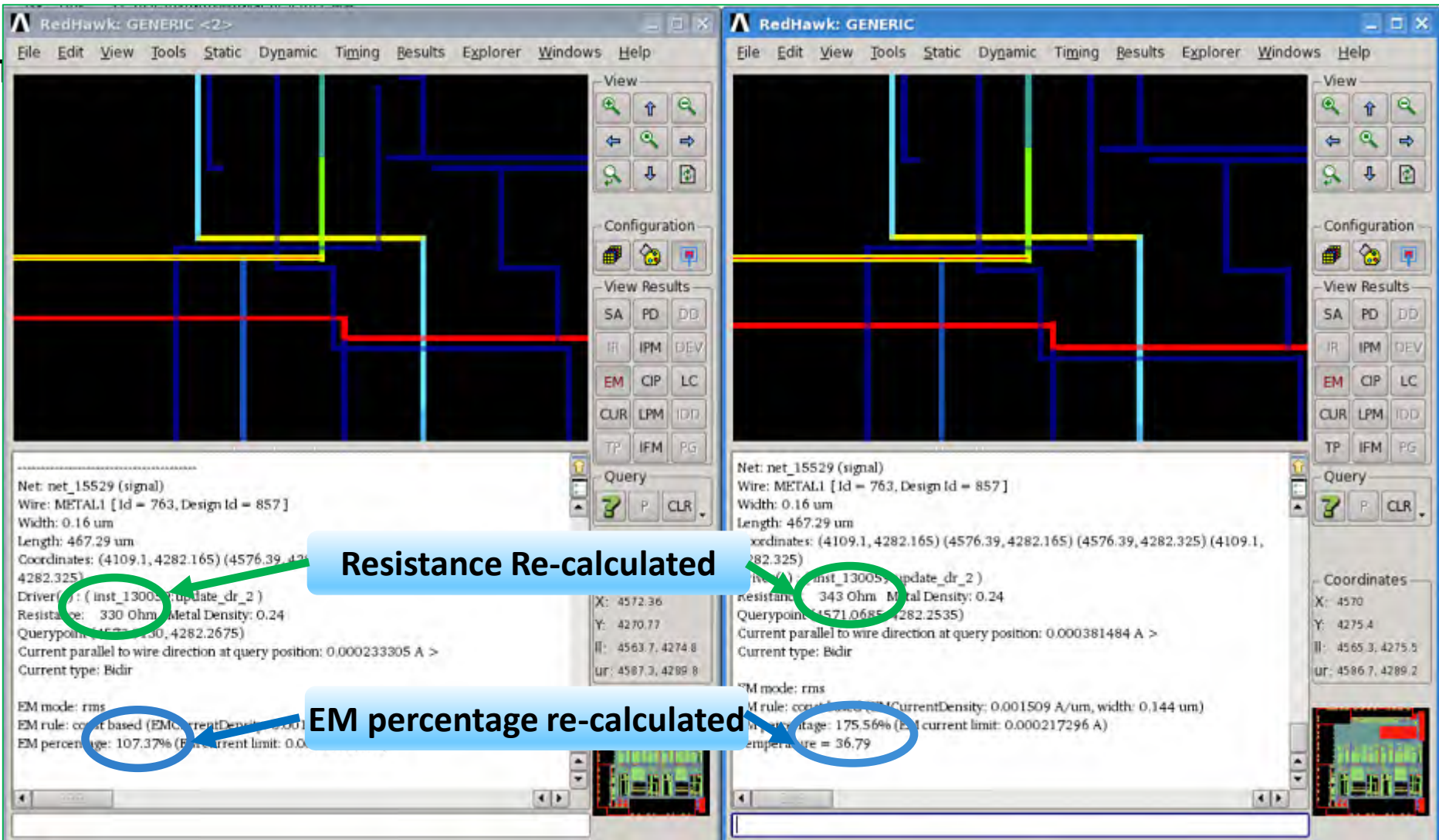
EM Color Maps



Tile-based temperature profile

- By layer EM color maps
- By layer temperature profile map

Redhawk Thermal-aware Resistance and EM vs. Package Design



Without Package Info

```

Net: net_15529 (signal)
Wire: METAL1 [Id = 763, Design Id = 857]
Width: 0.16 um
Length: 467.29 um
Coordinates: (4109.1, 4282.165) (4576.39, 4282.325)
Driver: ( inst_13005 update_dr_2 )
Resistance: 330 Ohm Metal Density: 0.24
Querypoint: (4576.39, 4282.2675)
Current parallel to wire direction at query position: 0.000233305 A >
Current type: Bidir

EM mode: rms
EM rule: cost based (EMCurrentDensity: 0.001509 A/um, width: 0.144 um)
EM percentage: 107.37% (EM current limit: 0.000217296 A)
                    
```

With Package Info

```

Net: net_15529 (signal)
Wire: METAL1 [Id = 763, Design Id = 857]
Width: 0.16 um
Length: 467.29 um
Coordinates: (4109.1, 4282.165) (4576.39, 4282.165) (4576.39, 4282.325) (4109.1, 4282.325)
Driver: ( inst_13005 update_dr_2 )
Resistance: 343 Ohm Metal Density: 0.24
Querypoint: (4571.0685, 4282.2535)
Current parallel to wire direction at query position: 0.000381484 A >
Current type: Bidir

EM mode: rms
EM rule: cost based (EMCurrentDensity: 0.001509 A/um, width: 0.144 um)
EM percentage: 175.56% (EM current limit: 0.000217296 A)
Temperature = 36.79
                    
```

Without Package Info

With Package Info



Demo Video

- **Show EM analysis with thermal effect**
- **Compare the comparison data between normal EM and thermal-aware EM**

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