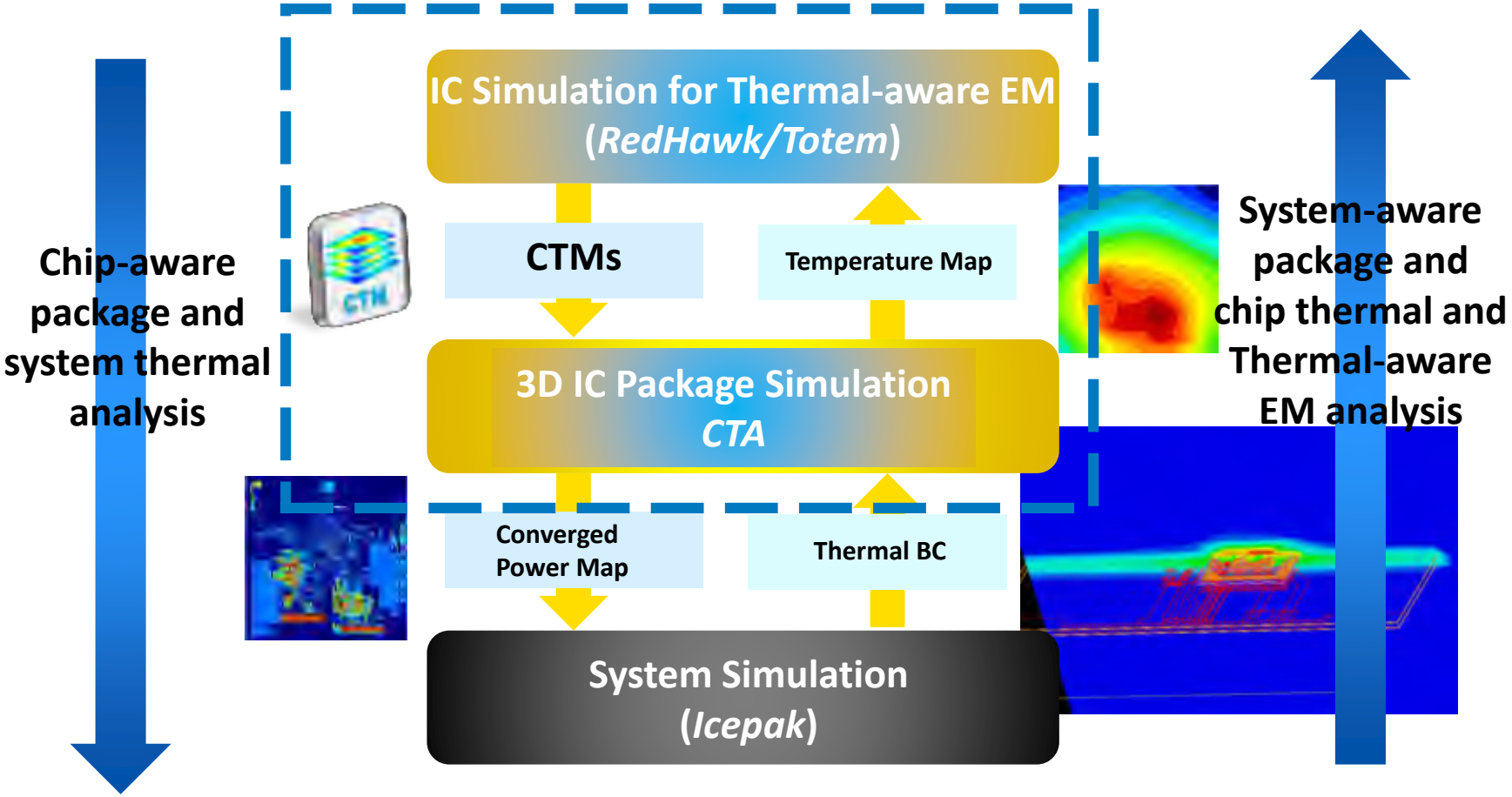
Chip Package System (CPS) Thermal Integrity Co-Analysis

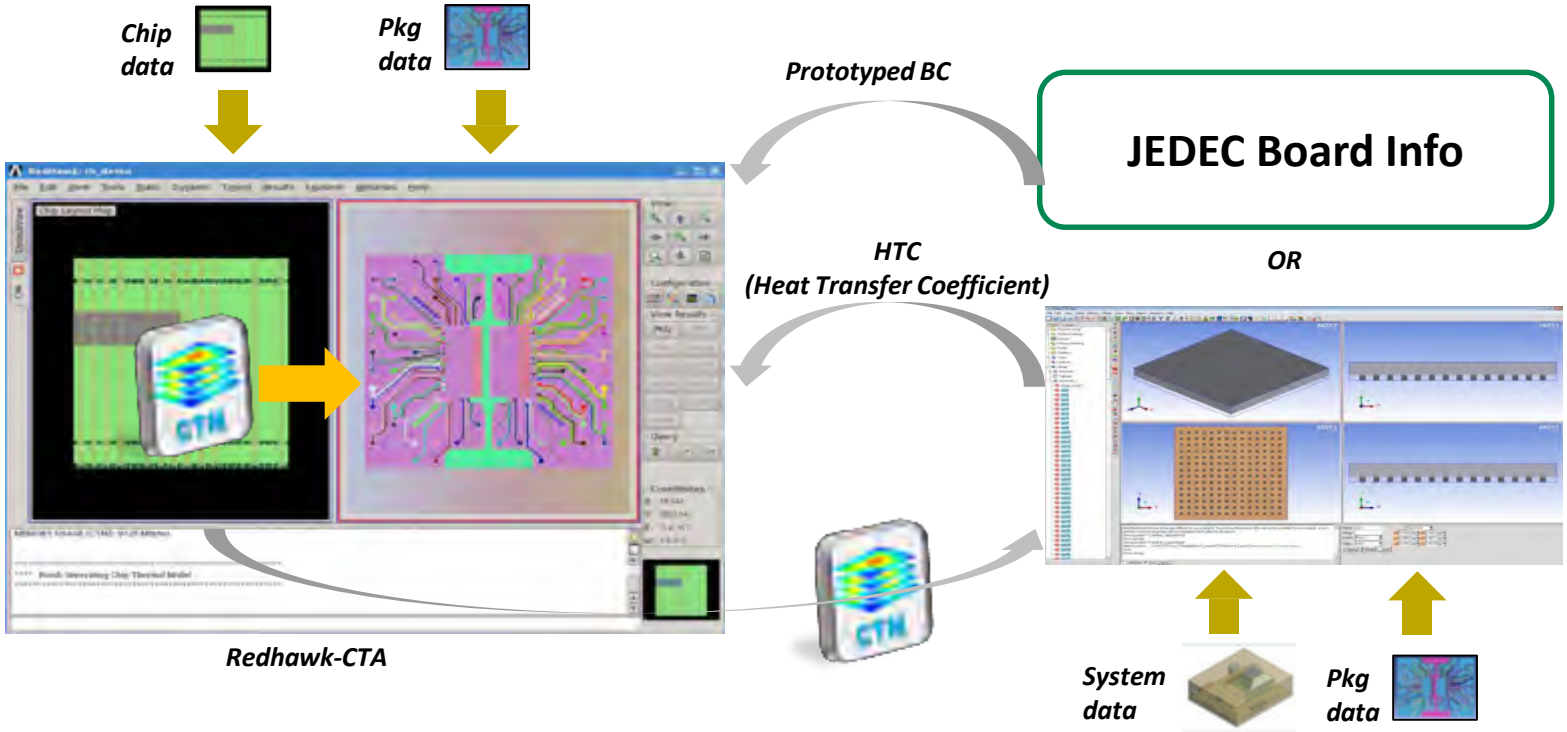
尹国丽/ Principal Product Specialist

Ansys

Chip-Package-System Thermal Integrity Solution



Chip & Board Aware Package Level Thermal Analysis

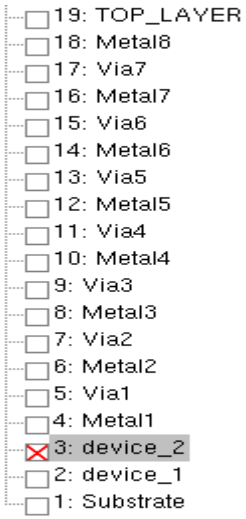


- JEDEC board is widely used for easy package level analysis when info about system is not ready or explicit

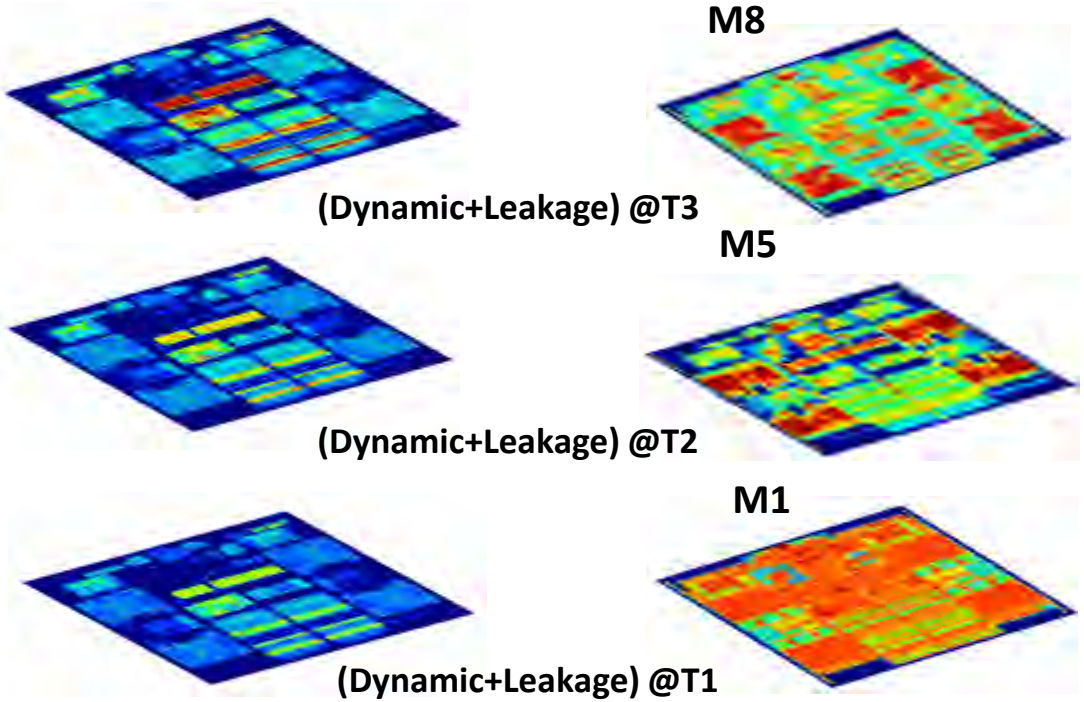
Chip Thermal Model (CTM) from RH/Totem

Layer stackup

Power (T)



Metal Distribution



CTM content

- Temp-dependent tile-based power density maps
- Per layer metal density map
- Block Power File (separate input)
  - OD and power info

Configuration File(GSR) Setting for Thermal Analysis

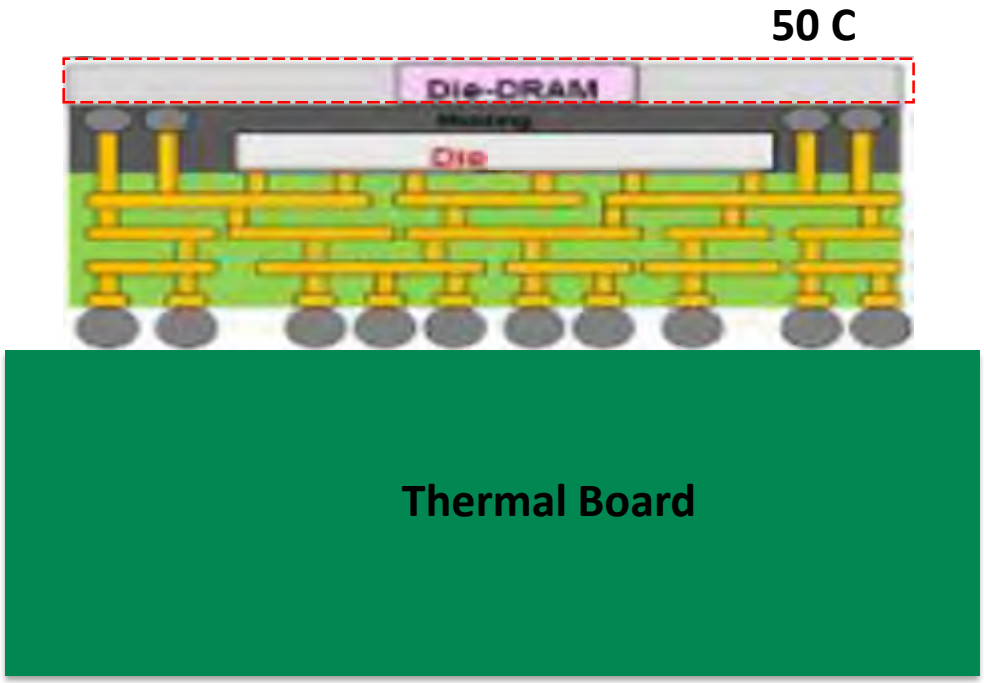
- **Specify Package Design and Result Directory**

```
CPA_FILES {
PACKAGE          ./design.mcm
MODEL            ./adsCTA
}
```

- **Must-have Option**

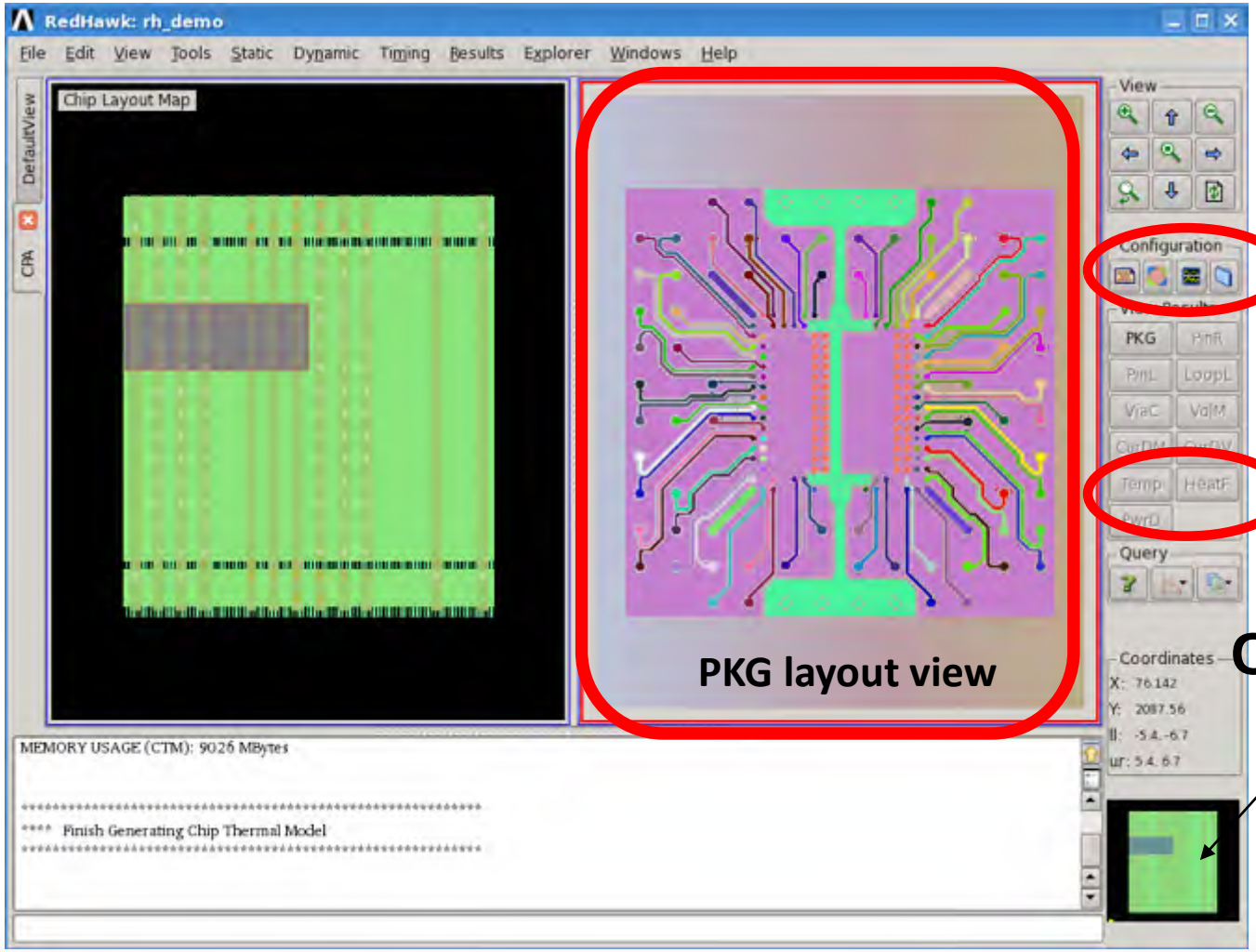
  THERMAL_ANALYSIS 1

Test Design Example: POP Design



- DRAM + Die + Interposer/Package + Thermal Board
- Prescribed temperature of 50C on DRAM
- CTM power maps on Die (from RH)

Invoke RedHawk/Totem-CTA

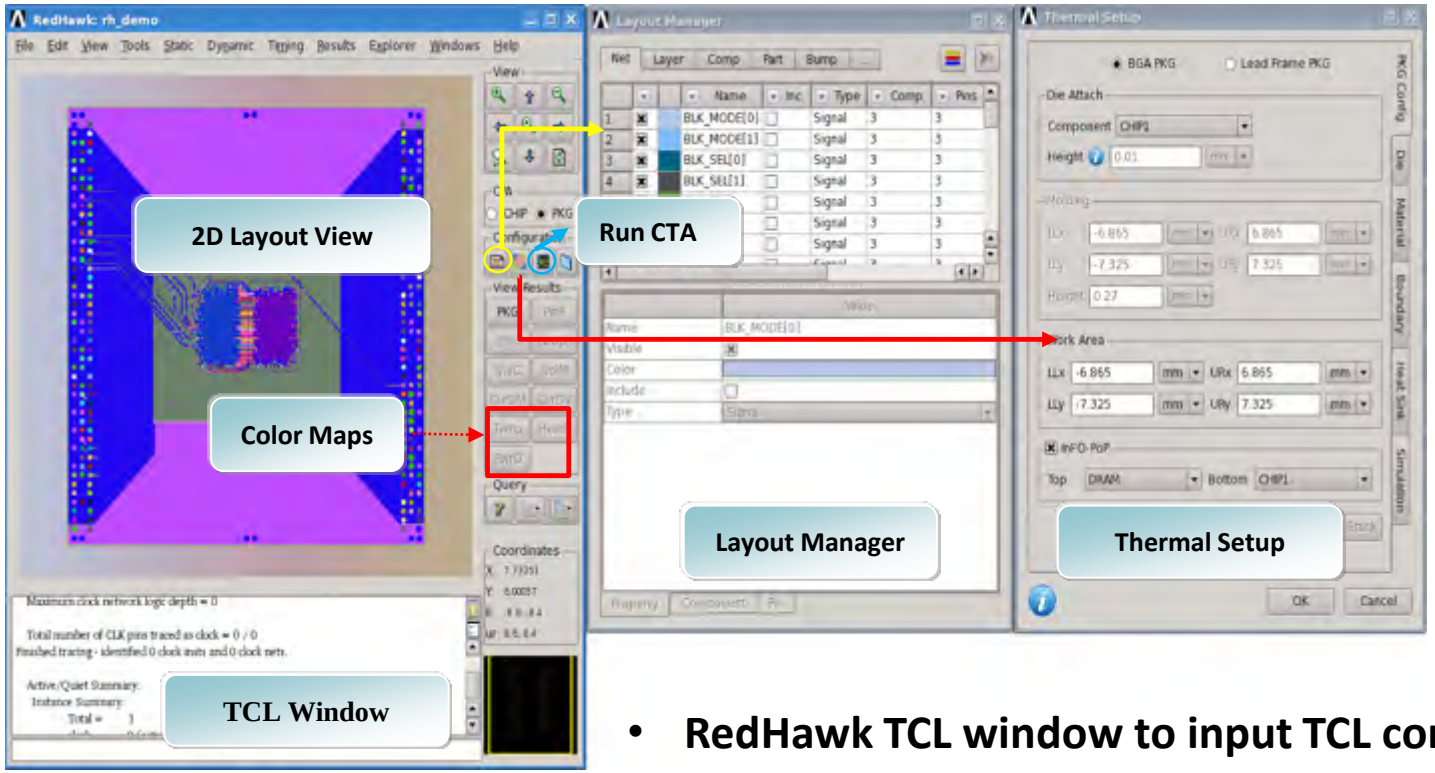


Geometry UI Setup

Color maps

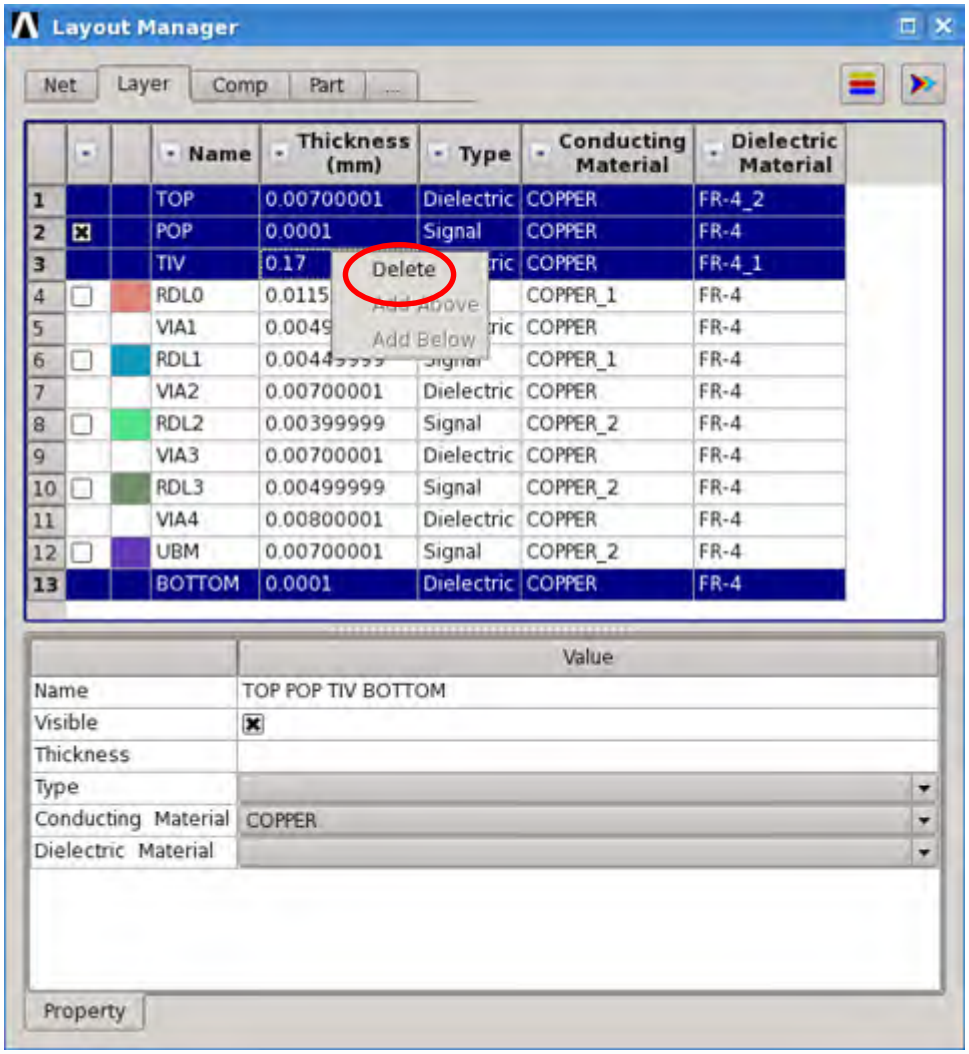
Chip Layout

Key Functions for Thermal Analysis



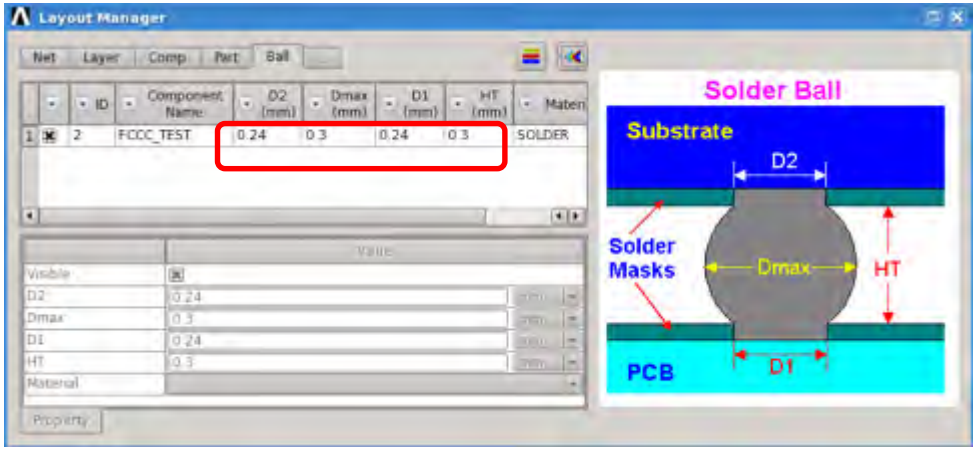
- RedHawk TCL window to input TCL commands
- Layout Manager for layout editing
- Thermal Setup dialog for all CTA setup
- Color Contours to Display Results

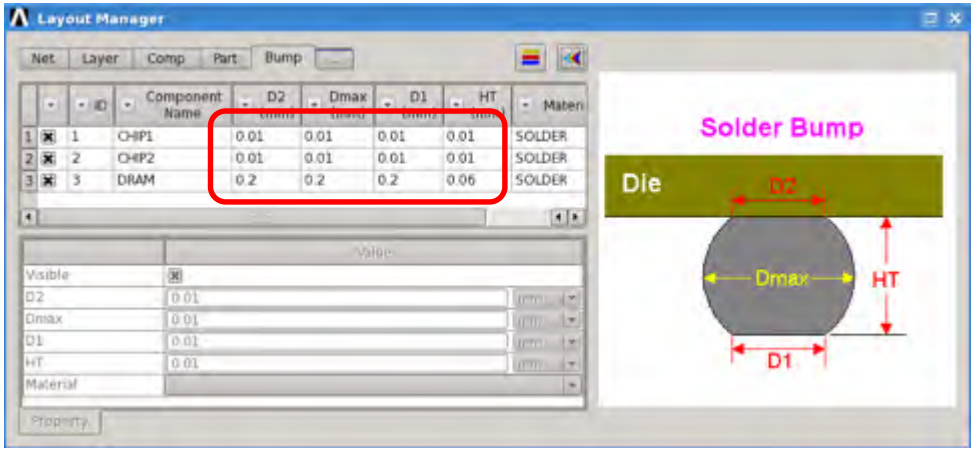
Design Setup through Layout Manager



- Set thickness, layer type conductive/dielectric material of target design
- Remove unnecessary layer info
- Various setting for design optimization through what-if analysis

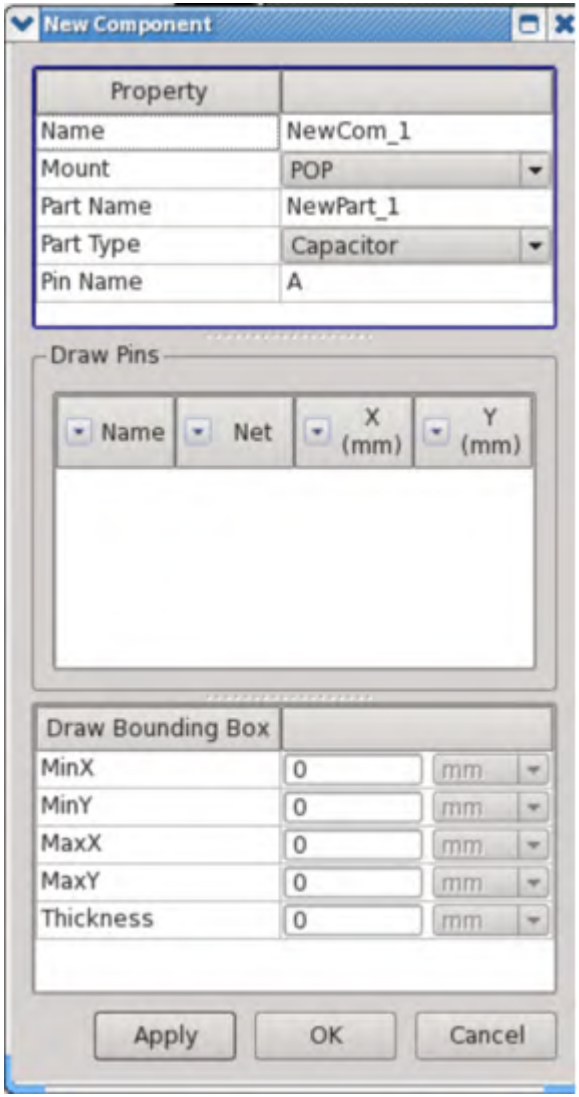
Specify Info for Bump/Ball

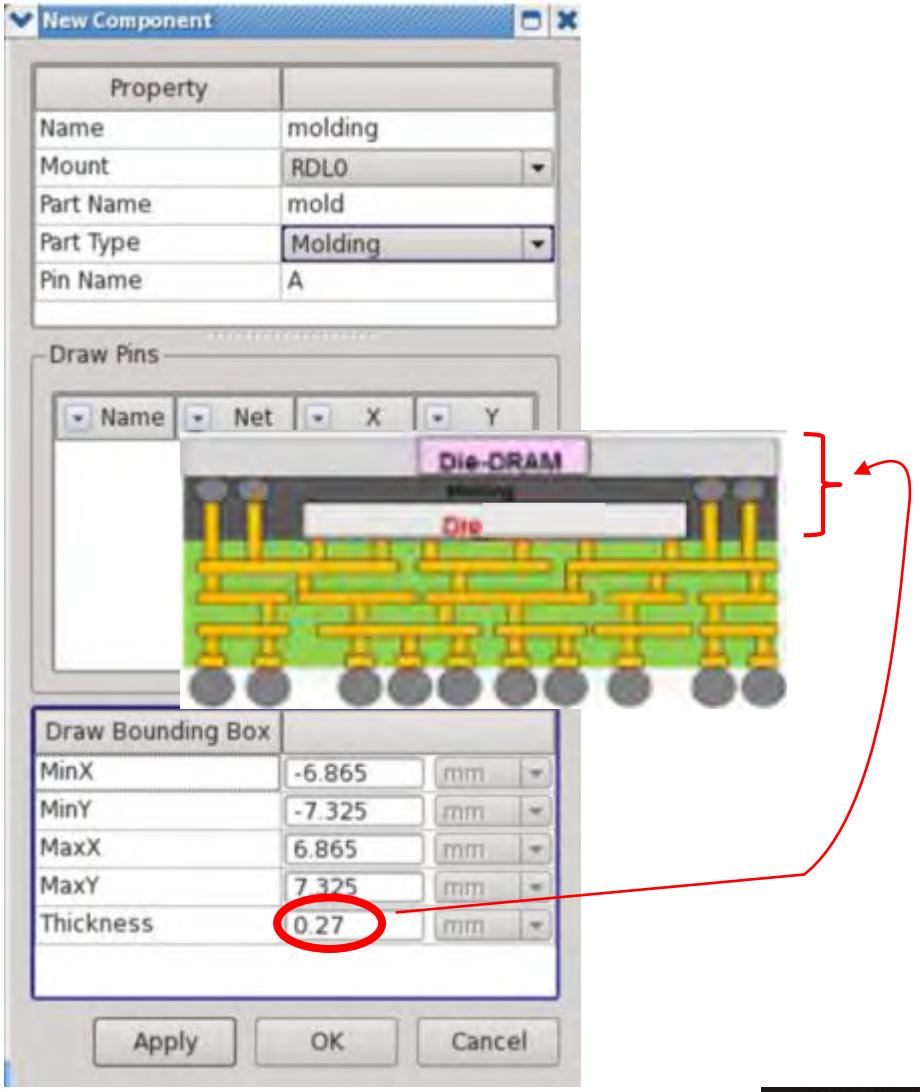




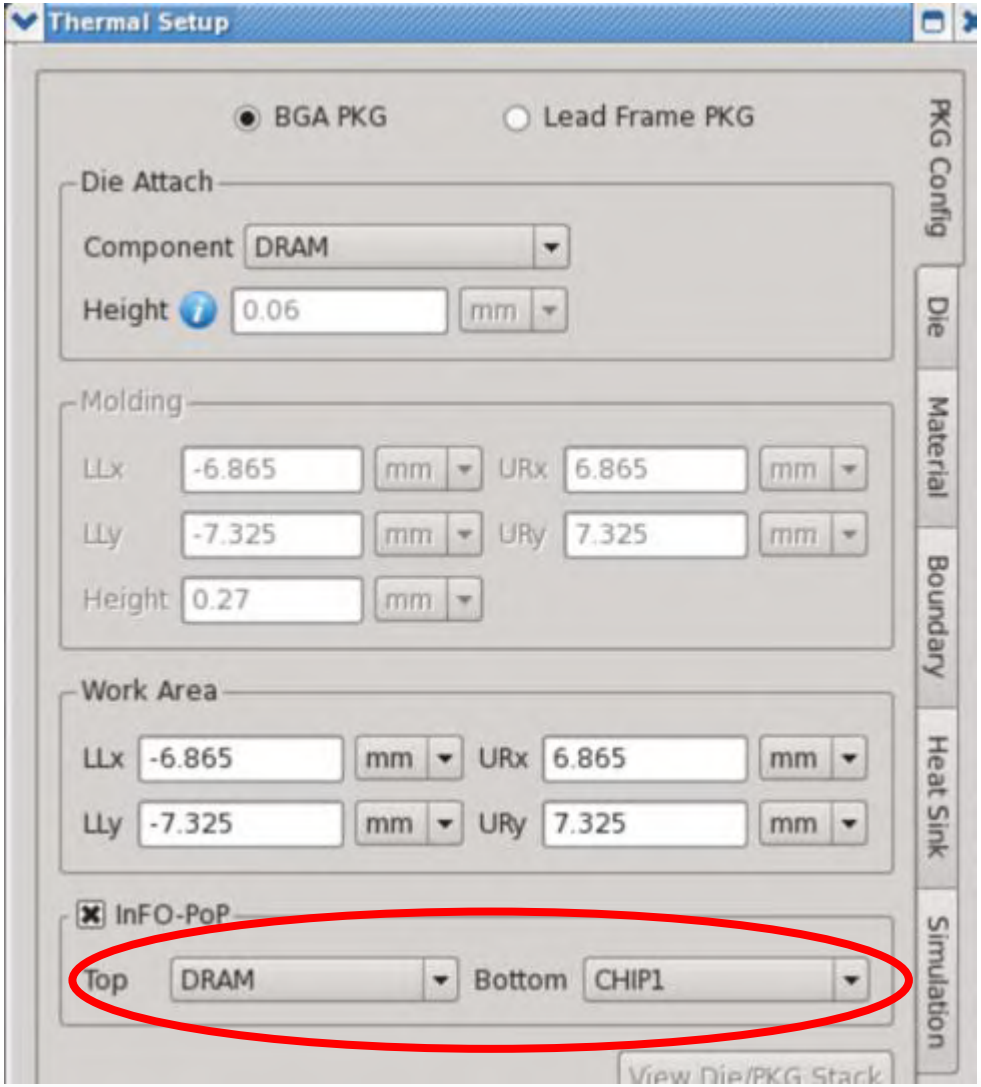
- Change Bump/Ball to practical values
- Bump/Ball are crucial info related to heat transferation

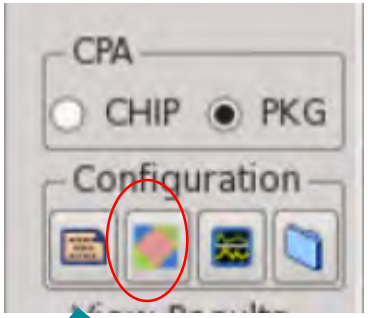
Add Molding to enclose Package and Die





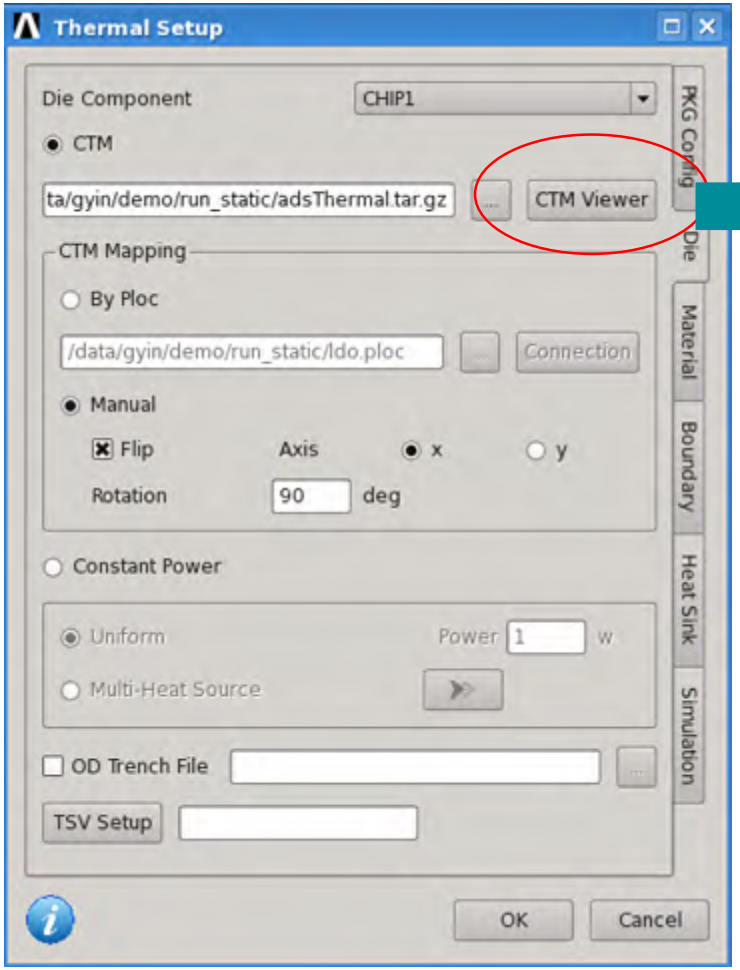
Set Up Package Configuration

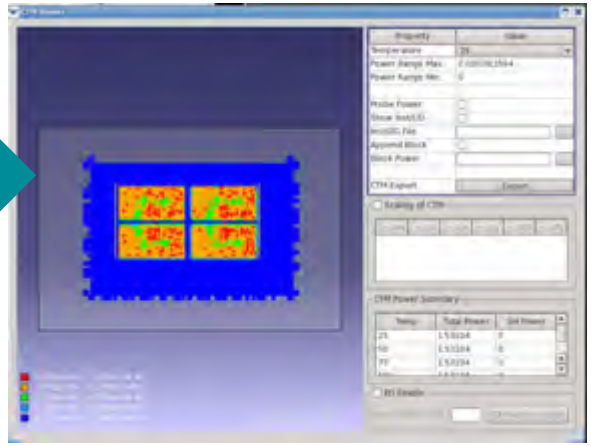




- **Stackup of DRAM on Die, i.e., DRAM on top of CHIP1**

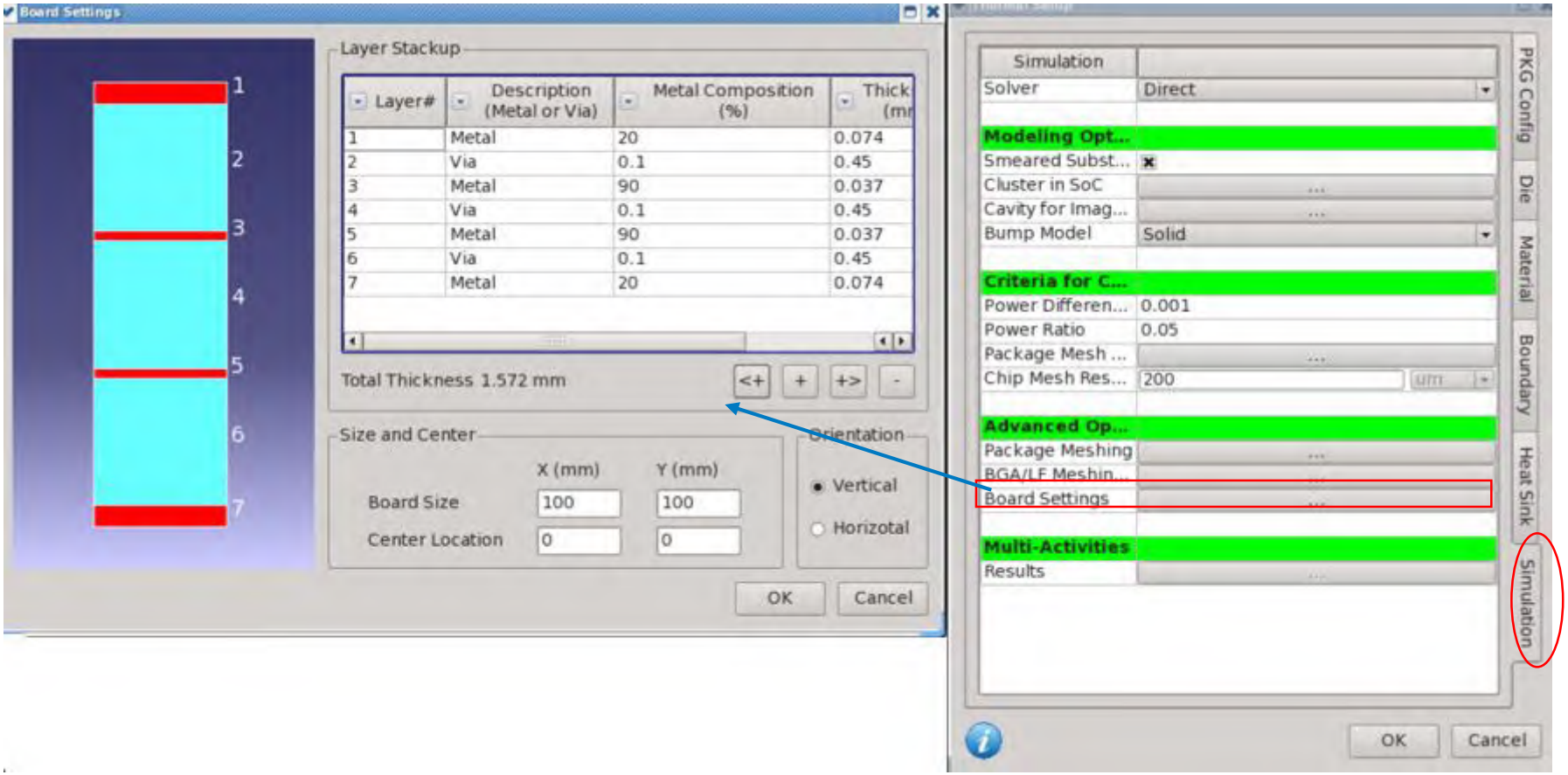
Heat Source Define: CTM, OD, Power Map



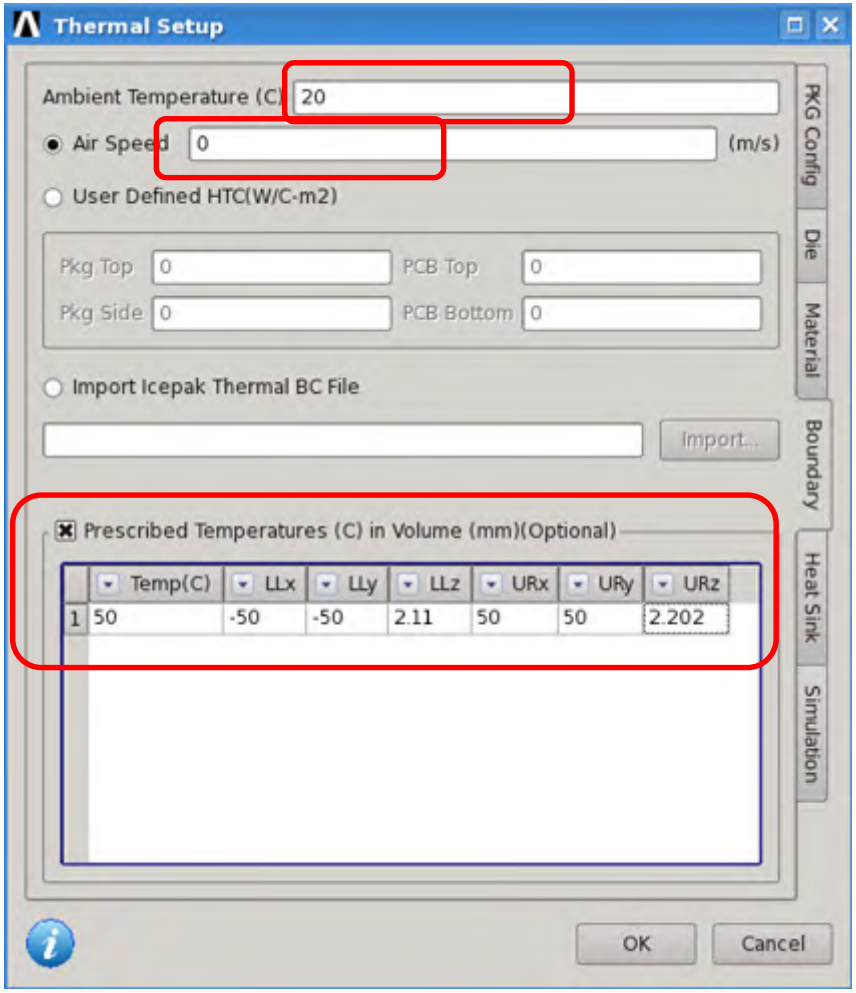


- For three die components, user needs to specify its CTM model or uniform power individually.
- If die adopts CTM power model, also specify its flip/Axis/rotation values to match package design and CTM power map

JEDEC Board Setting in RH-CTA

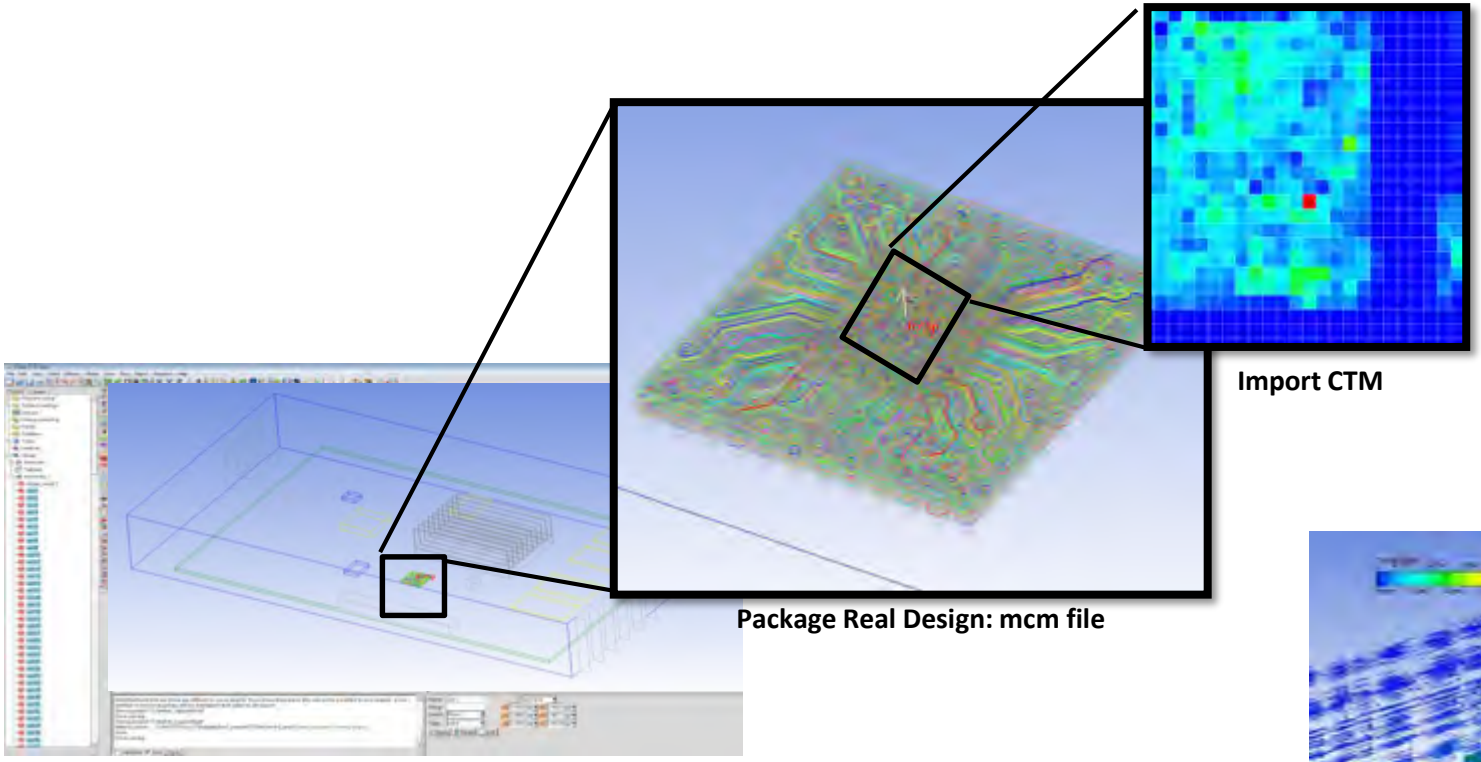


Thermal Boundary Condition(BC) Set up



- Import HTC from IcePak or User-defined
- User-defined setup example
  - Specify env temperature; default 20C
  - Specify Air speed 0;
  - Specify prescribed temperature on top of DRAM

HTC Generation from IcePak



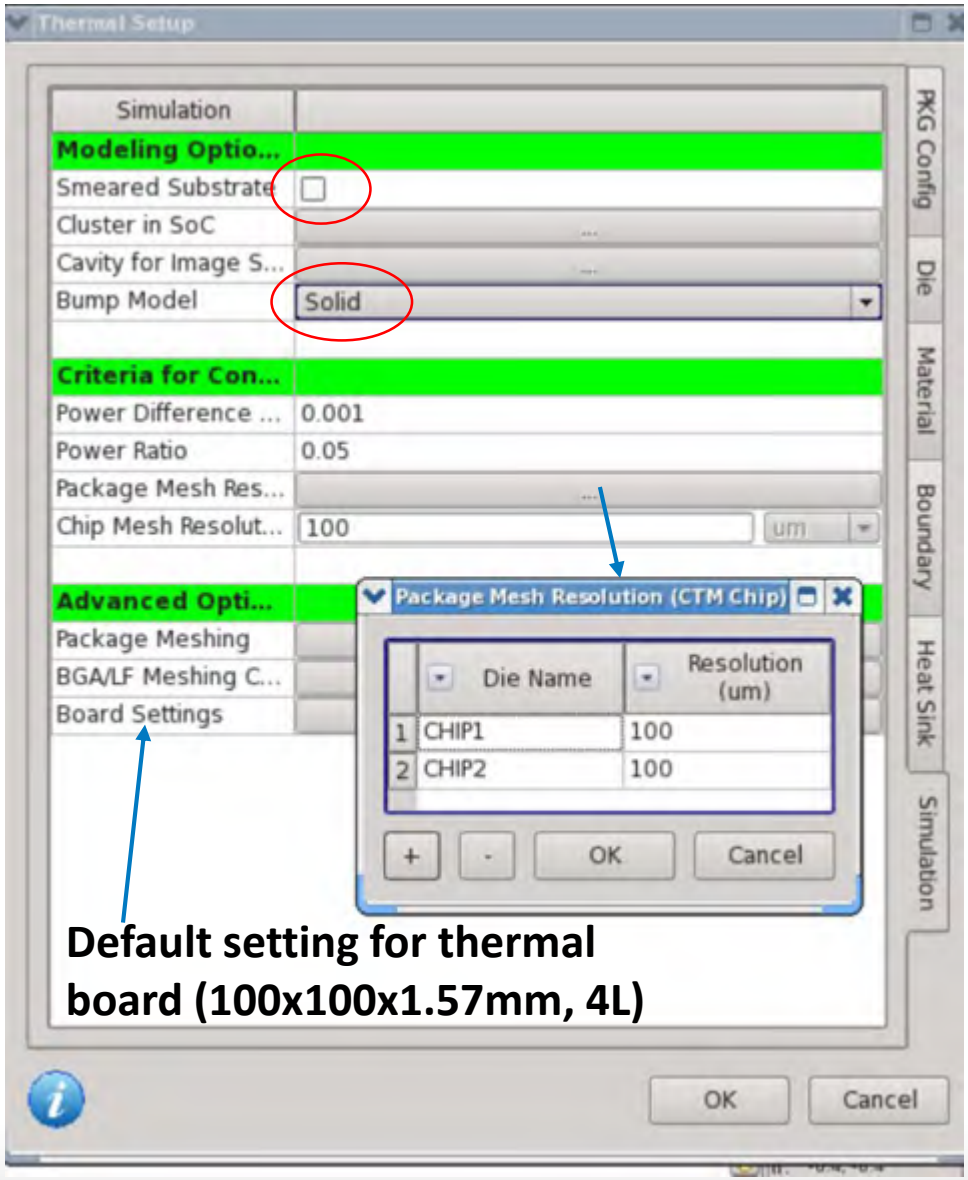
IcePak

Package Real Design: mcm file

Import CTM

HTC Generation

Simulation Configurations

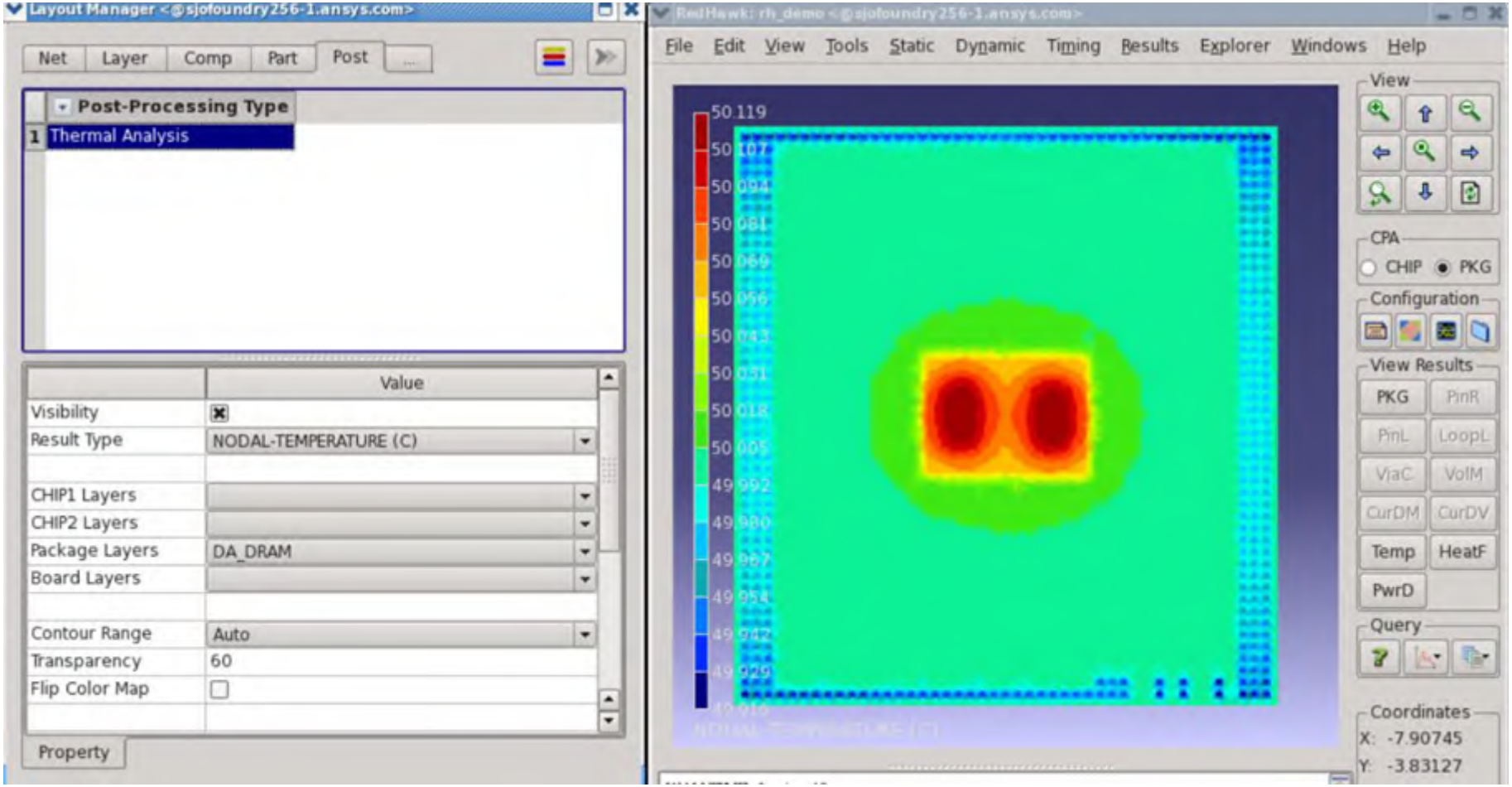


All layers modeled explicitly

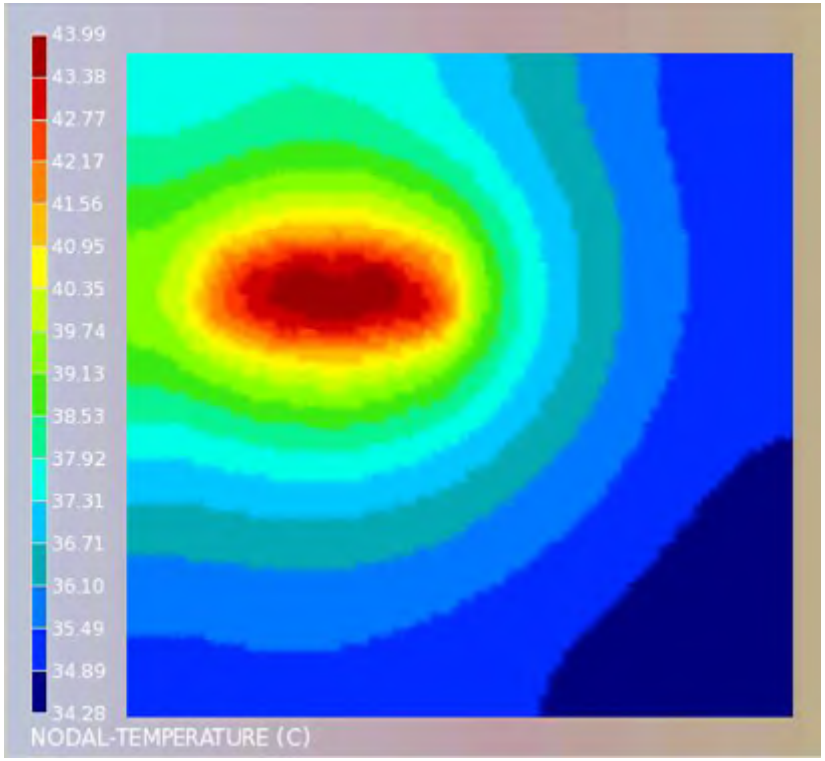
Solid elements for bumps/TIV

100um resolution for CTM dies

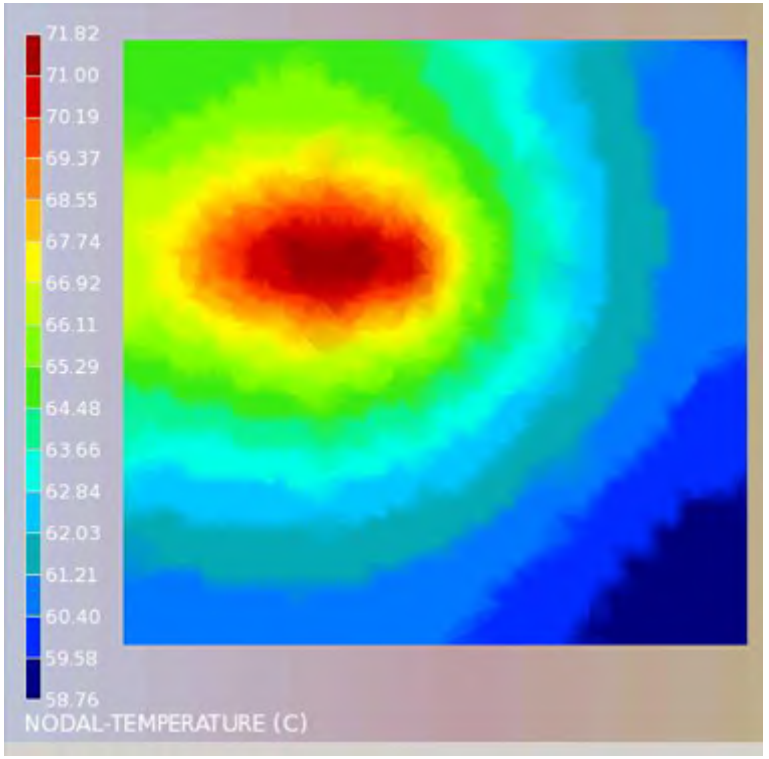
Thermal Analysis Results



Package Level Thermal Profile vs. Heat Source



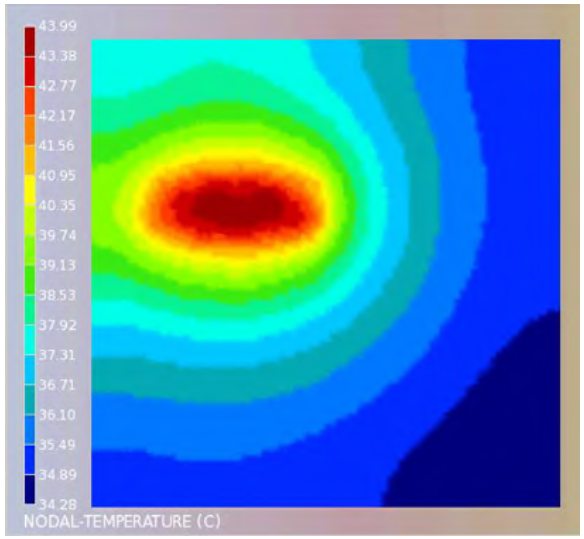
CTM(Chip Thermal Model)



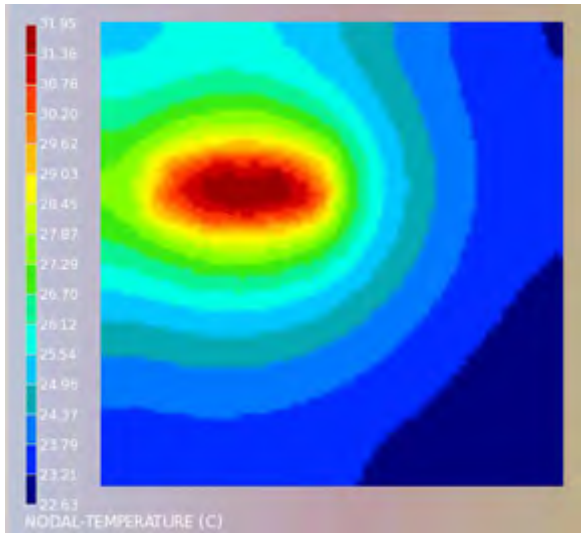
30x30 Bin-based Power Map

- Wrong power map can lead to a wrong temperature result

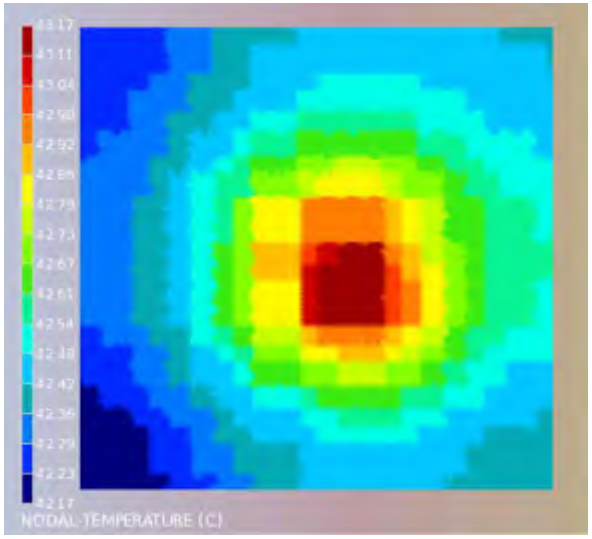
Package Level Thermal Profile vs. HTC



Without HTC



HTC based on Prototyped BC



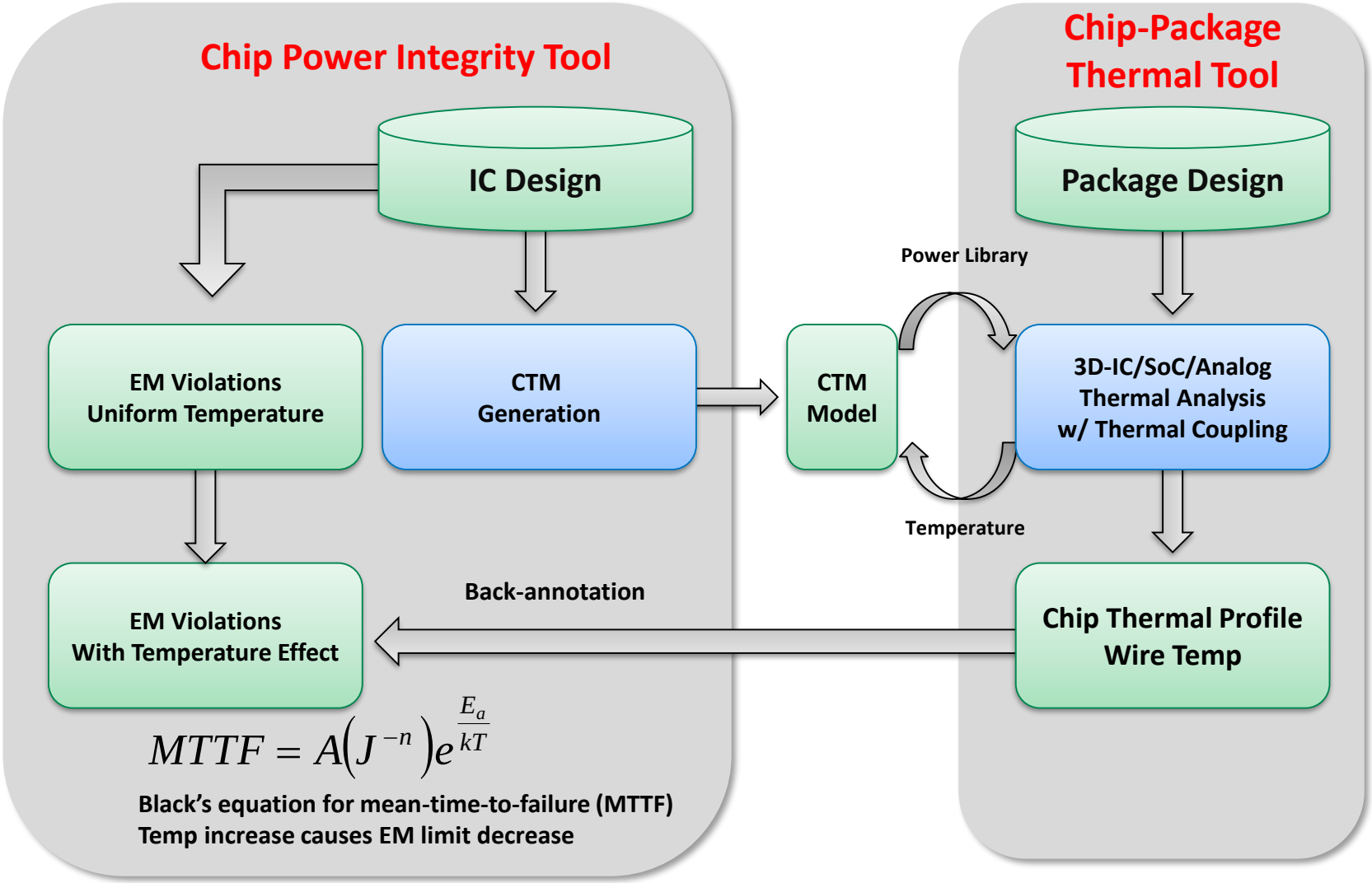
HTC from IcePak

- Hotspt and thermal profiles are different according to boundary condition and board design info
- CPS integrated solution is necessary for accuracy

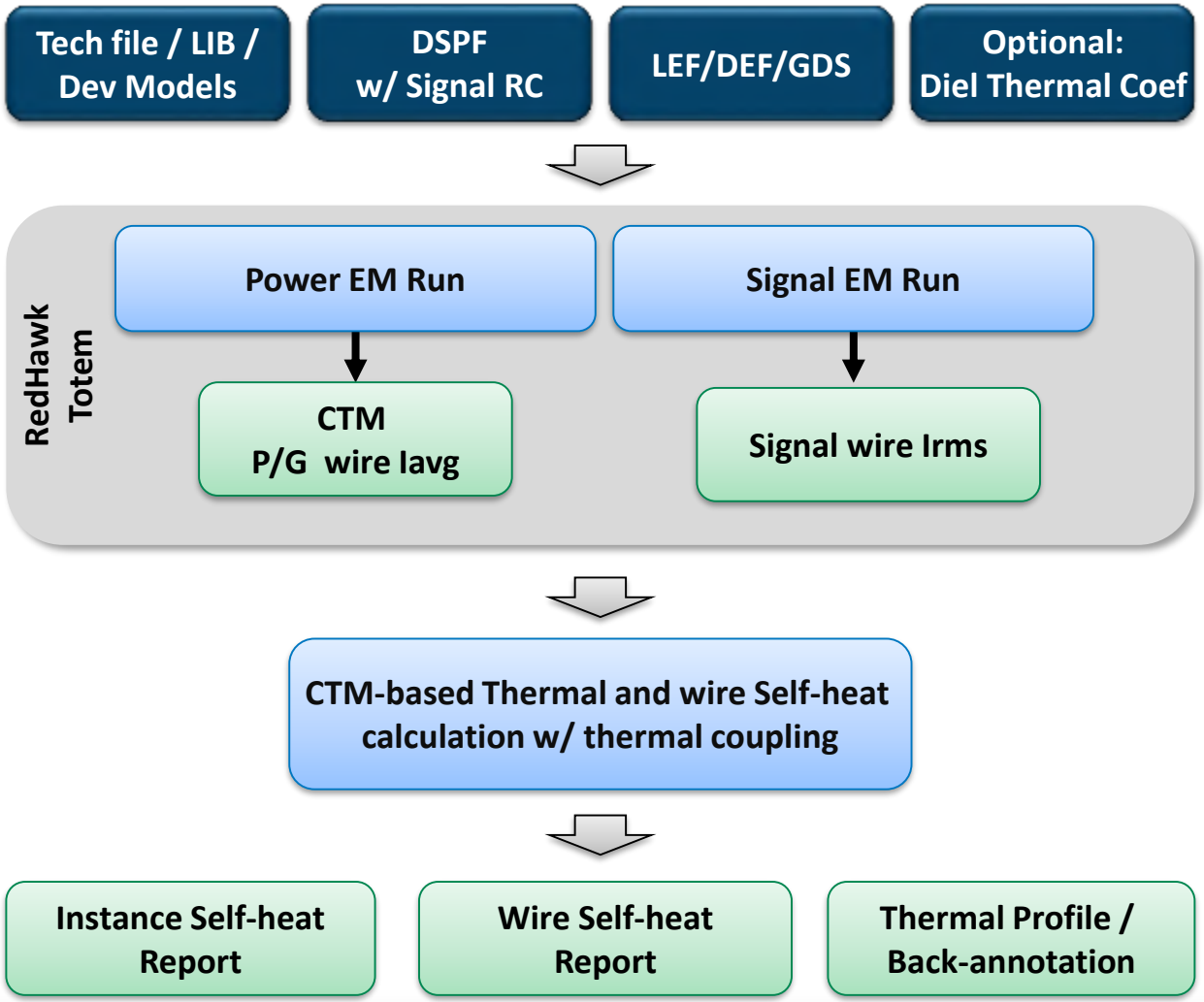
Demo Video

- **Should includes**
  - Design Set up for package level thermal analysis
  - CTM generation and import
  - Boundary condition and Jedec board setting
  - Thermal analysis and result show

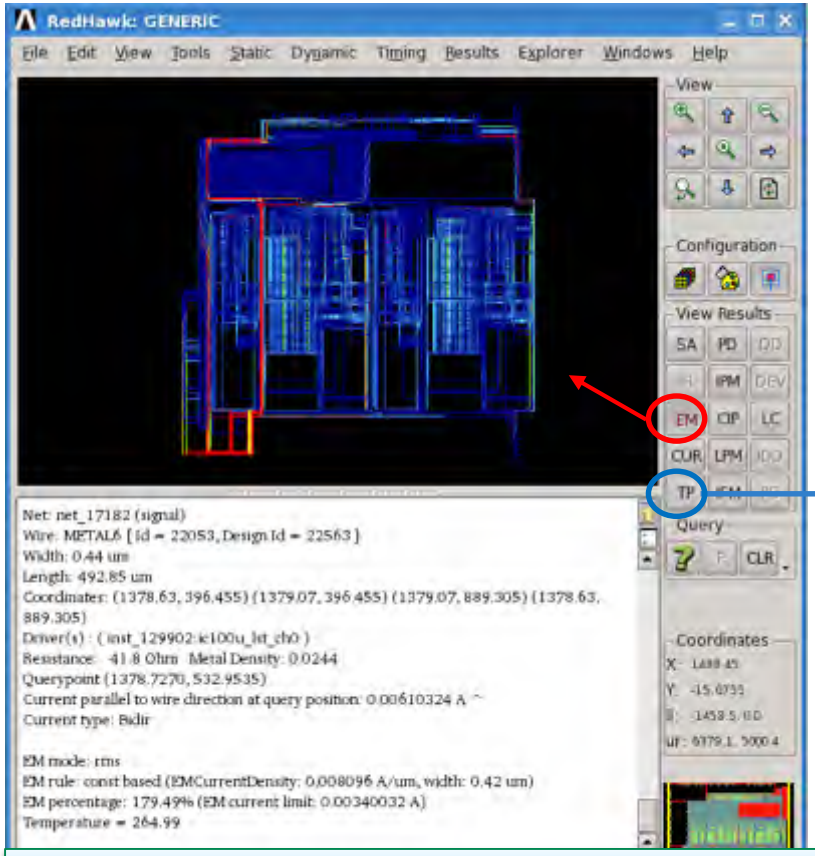
Chip-Package-System Thermal-Aware EM Flow

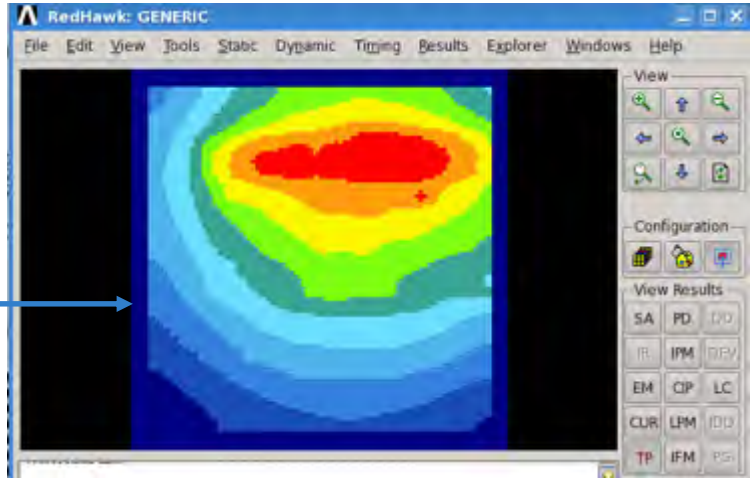


Self-heat Calculation Flow in RedHawk/Totem



RedHawk – View Thermal Maps



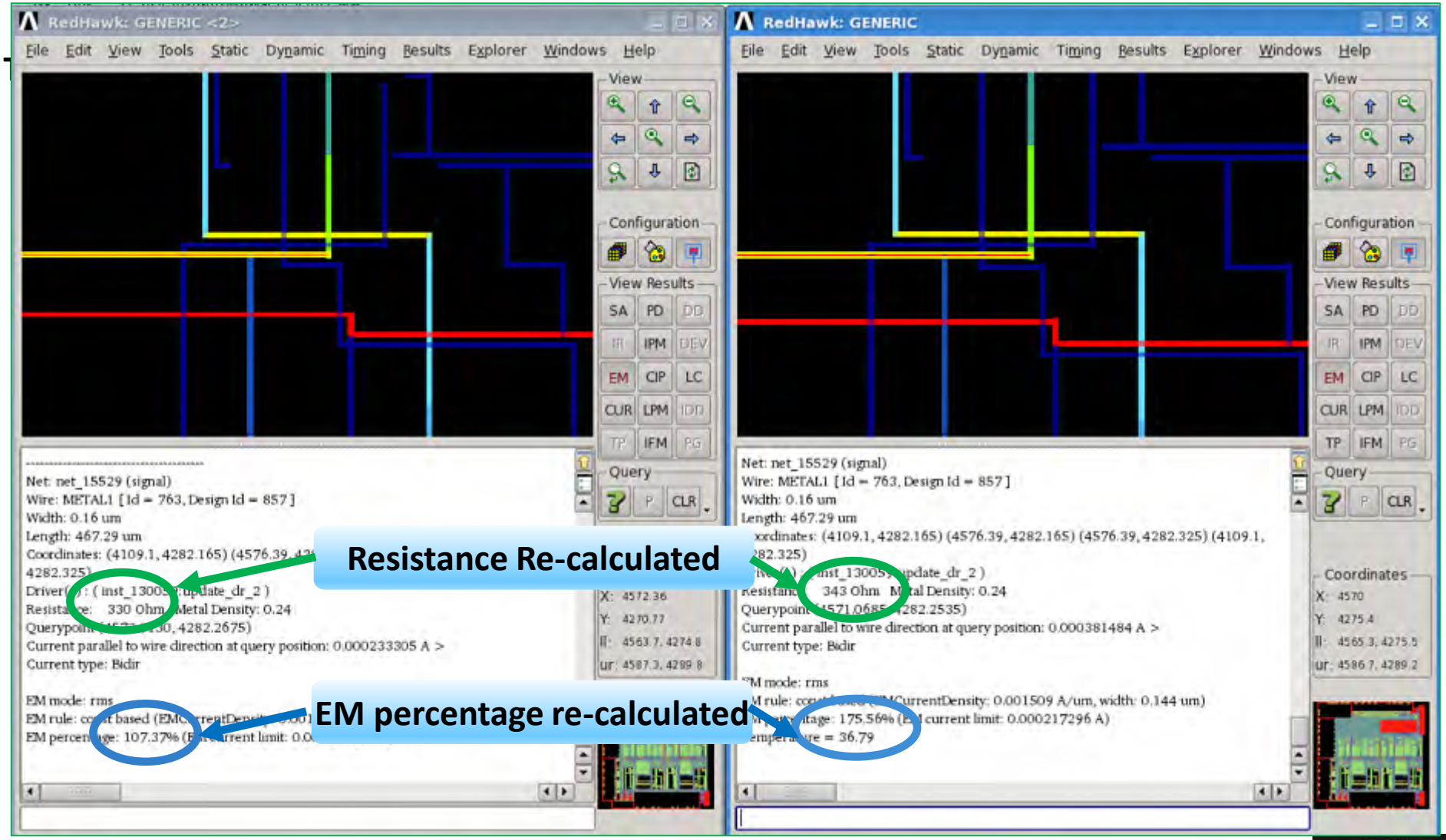


EM Color Maps

Tile-based temperature profile

- By layer EM color maps
- By layer temperature profile map

Redhawk Thermal-aware Resistance and EM vs. Package Design



Without Package Info **With Package Info**

Demo Video

- Show EM analysis with thermal effect
- Compare the comparison data between normal EM and thermal-aware EM

感谢聆听