Best EMC Practice of High Performance Electronic Device

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Summary

- **Far-Field EMI Analysis Methodology and Verification on SSD Boards**
- **Simulate with accuracy for high speed connector**

Far-Field EMI Analysis Methodology and Verification on SSD Boards

Contents

Trends of Data Storage

- **Hard Disk Drive (HDD) ➔ Solid-State Drive (SSD)**
  - ***Higher*** **read/write rate,** ***Faster*** **access time,** ***Lower*** **power consumption**

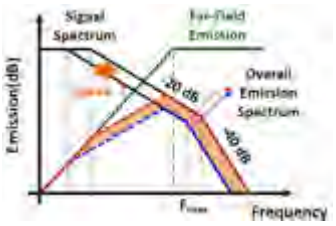
Source: www.google.com

Source: www.samsung.com

		SSD	HDD	Different
Media		NAND FLASH	Magnetic Platters	
Read/Write Speed	Sequential [MB/s]	540 / 330	60 / 160	X 9 / 2
	Random [IOPS*]	98000 / 70000	450 / 400	X 217 / 175
Data Access Time [ms]		0.1	10~12	X 100~120
Power Consumption	Active(Idle) [W]	0.127(0.046)	1.75(0.8)	X 13 ↓(X 17 ↓)

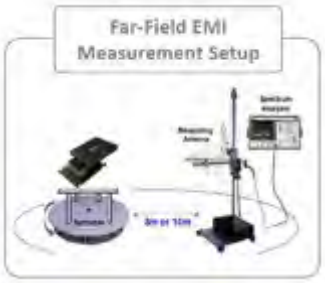
Potential EMI Risk in SSD Products

- ***Speed*** **and** ***density*** **are continuously increasing ...**



Source: High-speed digital system design

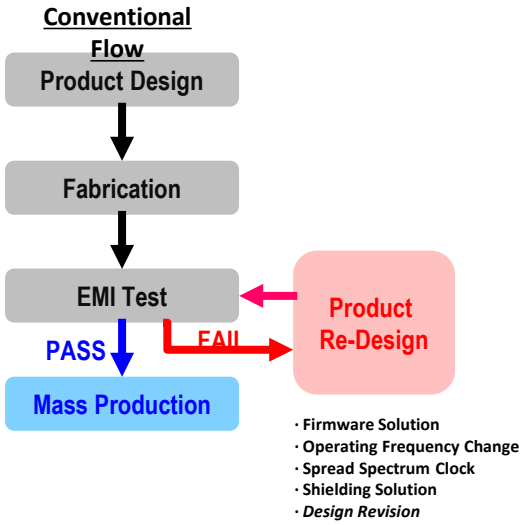
Source: www.google.com

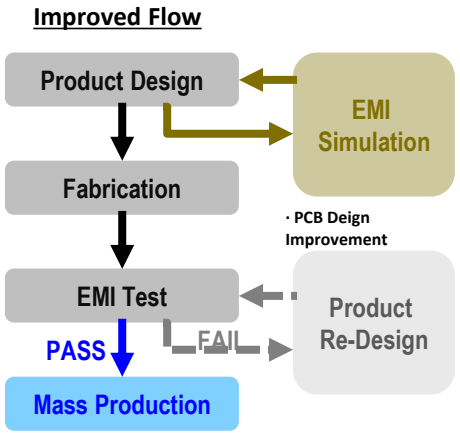


Electromagnetic interference (EMI) becomes a critical issue !

EMI Simulation Methodology

- **Measurement-based EMI verification requires additional *cost* and *time* to debug**

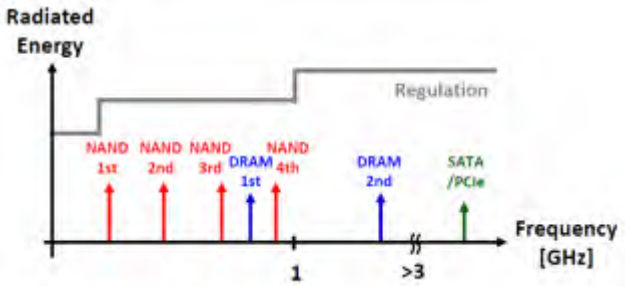




EMI Noises in SSD Products

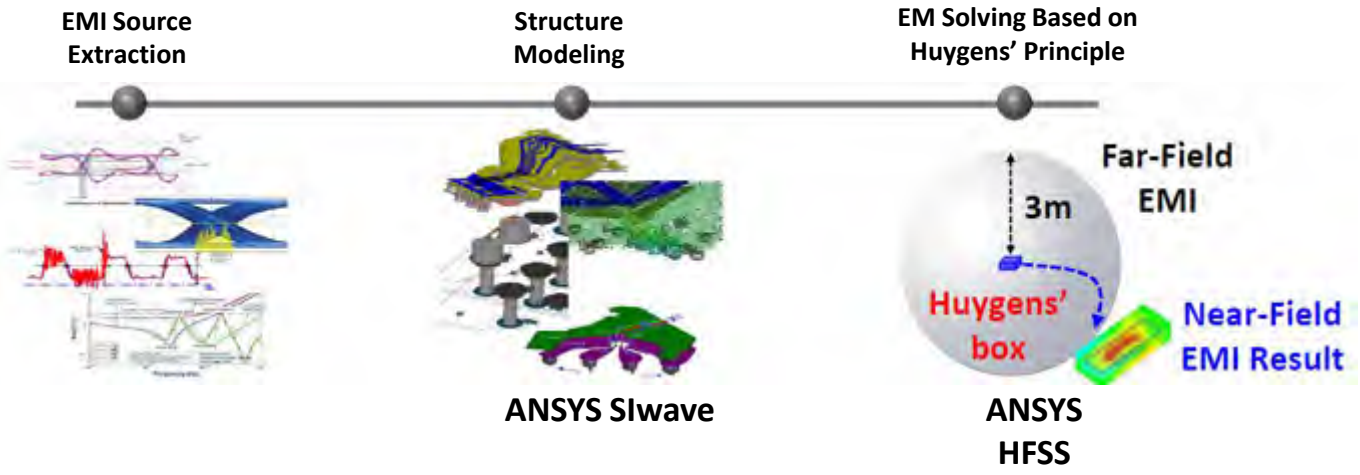
- **Various devices in SSD**
  - **NAND, DRAM, Controller, PMIC, ...**
  - **Operated with different speed and voltage**
- **Interfaces**
  - **DRAM ↔ Controller Interface**
  - **Controller ↔ Host interface**
  - **NAND ↔ Controller Interface**
  - **- Higher supply voltage, Longer board routing**

Source: www.samsung.com



Proposed Far-Field EMI Simulation Flow

- **Far-field EMI simulation methodology [Ref. APEMC2015, Benson Wei et. Al.]**
- **Propose 3 items to enhance simulation *accuracy* and *efficiency***
  - EMI source extraction
  - Package and reference plane modeling
  - Huygens' box optimization for near- to far-field transform

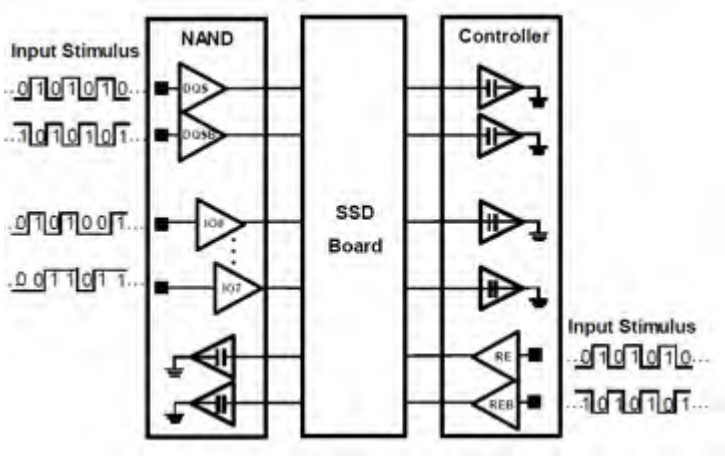


Stage 1: EMI Source Extraction

- **Read operation at 460 Mbps**

  (NAND ↔ controller interface)

- **Block diagram**
  - NAND Flash I/O buffer
  - Controller I/O buffer
    - SSD board model (S-parameter)
- **Input stimulus**
  - Data: PRBS 27-1
  - Strobe/clock: periodic pattern



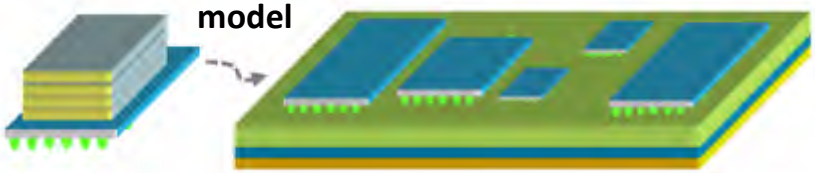
(5% duty cycle for power noise modeling)

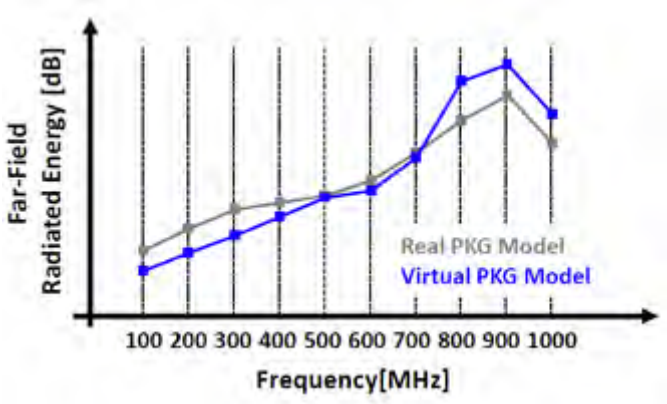
Stage 2: Structure Modeling (1)

- **EM simulation with package and board together**
  - **Impractical solution due to simulation time and hardware resources**
- **Propose virtual package model with metal plane**

***Real* PKG model**

***Virtual* PKG model**

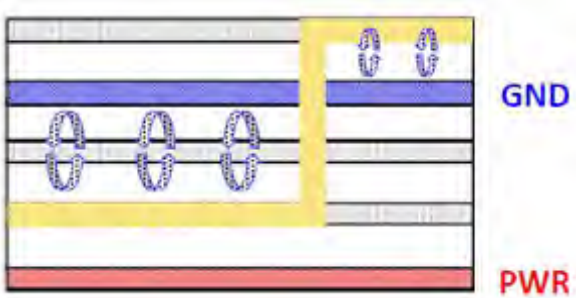




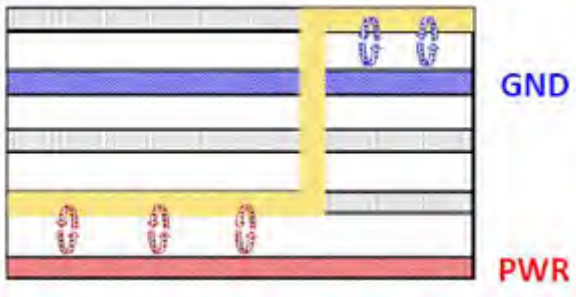
Both simulation results have similar tendency

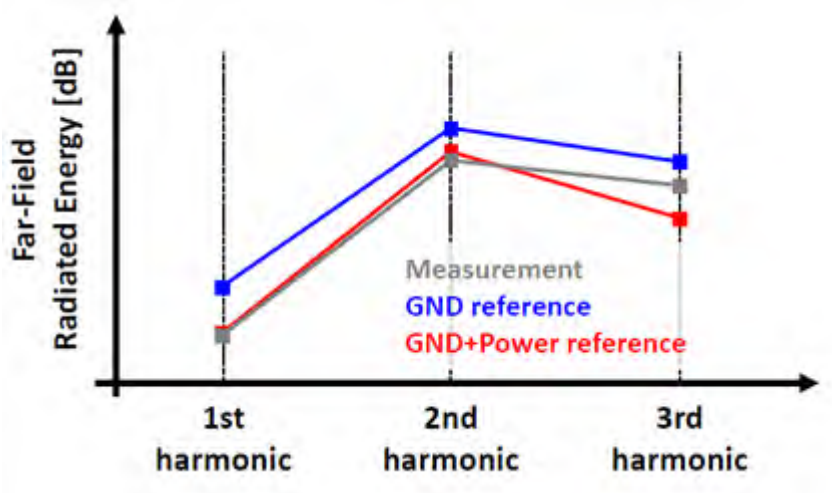
Stage 2: Structure Modeling (2)

Ground Reference



Power /Ground Reference



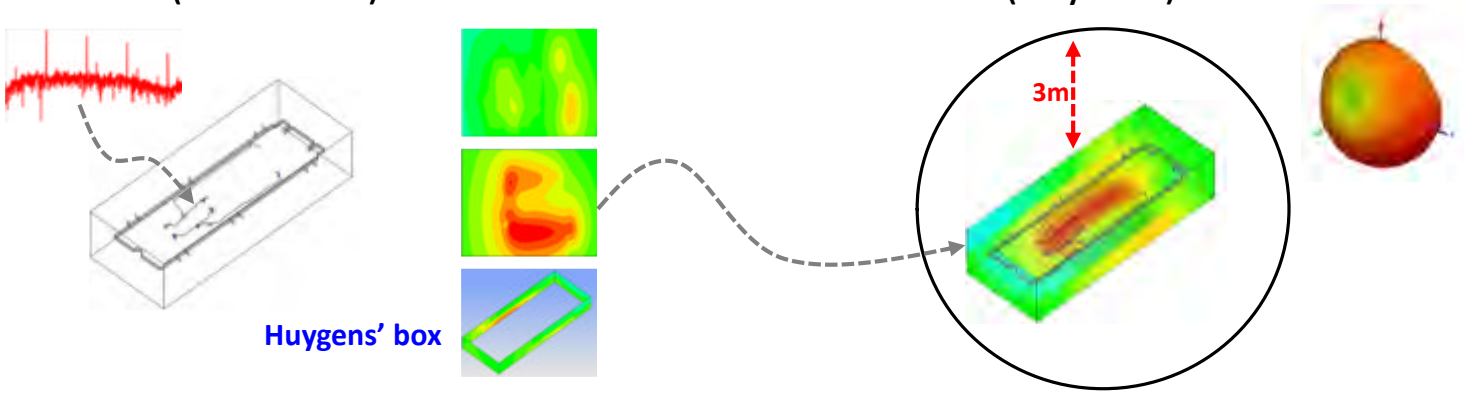


Stage 3: EM Solving Based on Huygens' Principle

- Near- to far-field transform method based on Huygens' principle
  - Radiated energy simulation at 3-m distance from micro-unit SSD board

N/F Simulation – 2.5D EM solver (ANSYS SIwave)

F/F Simulation – 3D EM solver (Ansys HFSS)



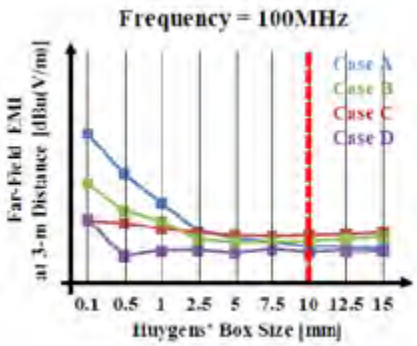
Attach I/O current as EMI source

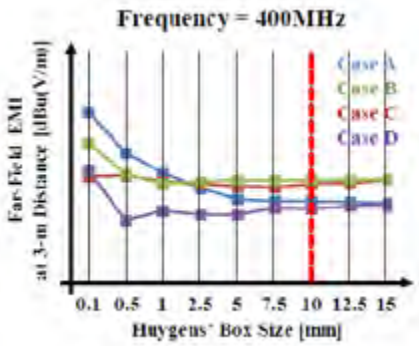
Maximum electric field calculation at 3-m sphere surface

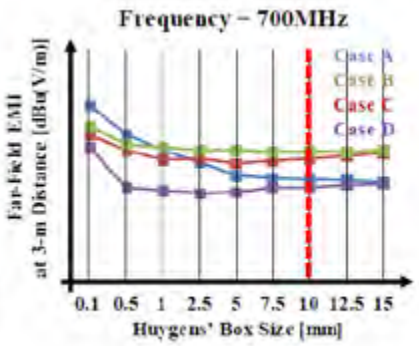
How to optimize Huygens' box size?

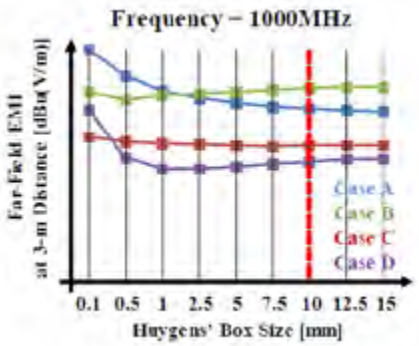
Stage 3: EM Solving Based on Huygens' Principle (cont'd)

- **Huygens' box size optimization**
  - **Optimized box size is necessary to minimize simulation error for near- to far-field transform**
  - **Radiated field is saturated from *10-mm* box size**



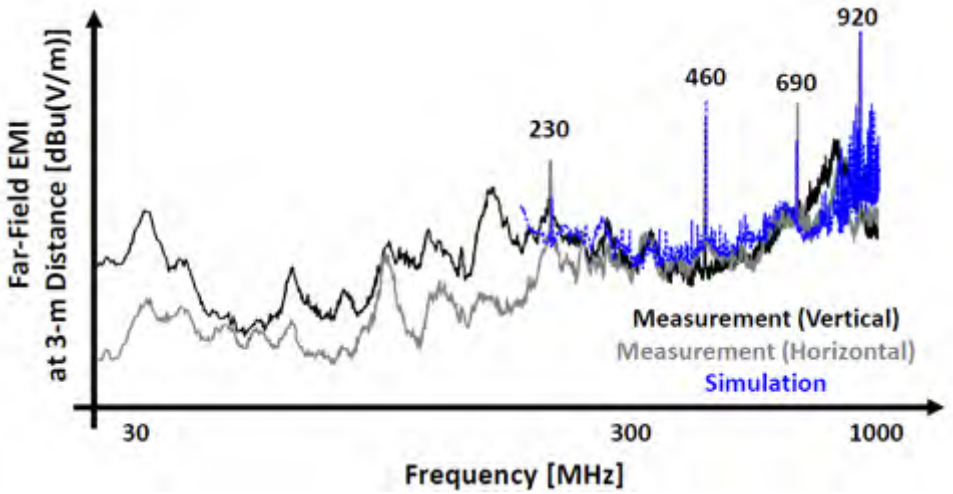






Correlation with Far-Field Measurement Results

- Read operation at 460 Mbps (NAND ↔ Controller Interface)
- Good agreement up to 1GHz between *simulation* and *measurement* results

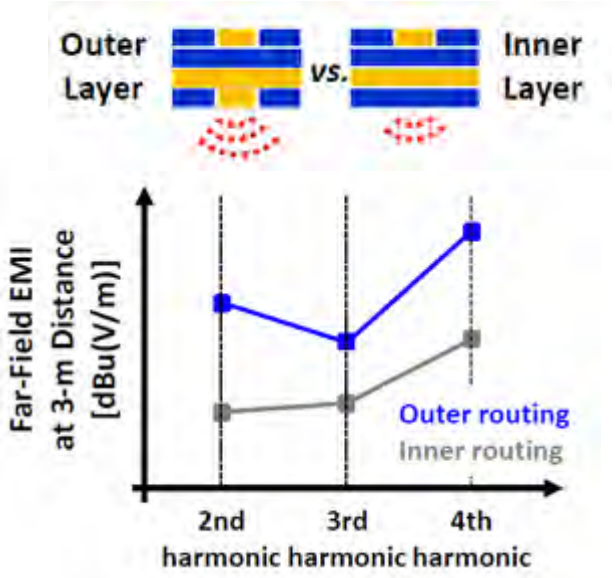


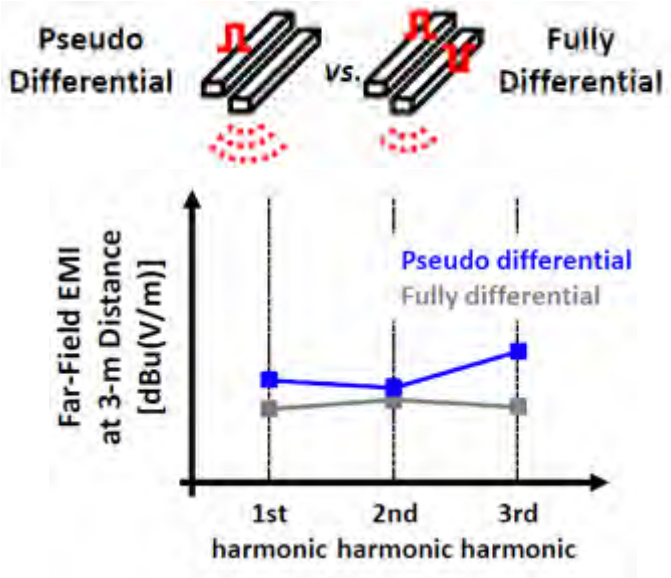
Measurement (Vertical)

Measurement (Horizontal)

Case Analysis (1)

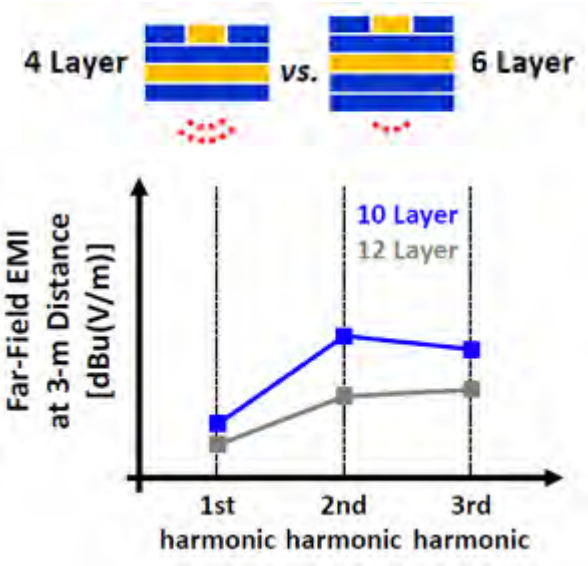
- **Relationship between board design and far-field EMI**
  - **Routing scheme: Inner layer < Outer layer**
  - **Signalling scheme: Fully differential < Pseudo differential**

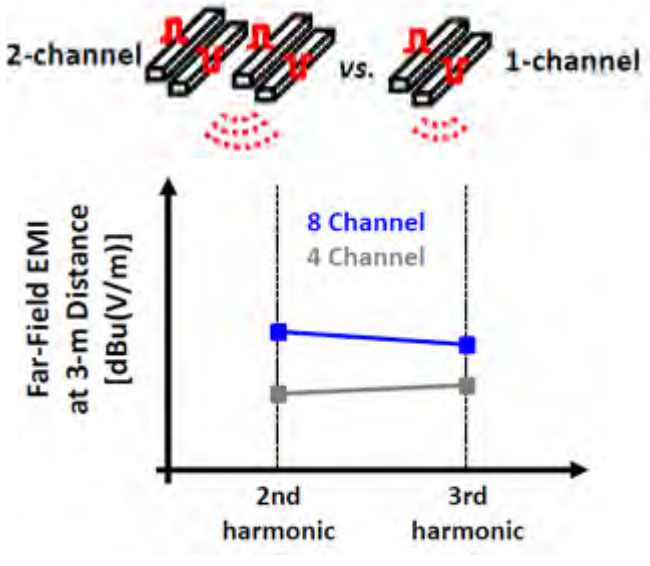




Case Analysis (1)

- **Relationship between board design and far-field EMI**
  - **Number of layer: 12 layer < 10 layer**
  - **Number of channel: 4 channel < 8 channel**





Conclusion

- **Far-Field EMI Simulation Methodology on Commercial SSD Products**
  - **EMI source extraction**
  - **PCB structure modeling**
  - **EM solving method based on Huygens' principle**
- **Good Correlation Between Simulation and Measurement Results**
- **Relationship Between Board Design and Far-Field EMI**
  - **Routing scheme, signal scheme, number of board layer and channel**
- **EMI Analysis in the Design Stage Prior to the Manufacturing Process**

Simulate with accuracy for high speed connector

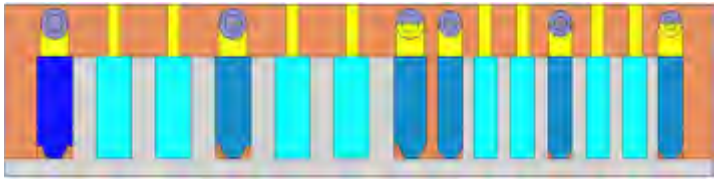
Objective

- Correlate simulation and measurement data of customized Molex SAS-3 plug 78695 mated with Molex SAS-3 receptacle.
- Both Differential S parameter and TDR are extracted for correlation.

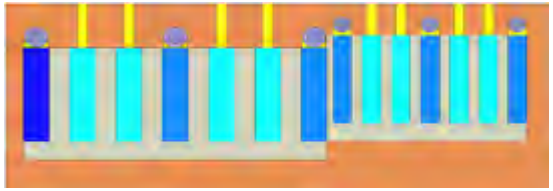
Connector Used

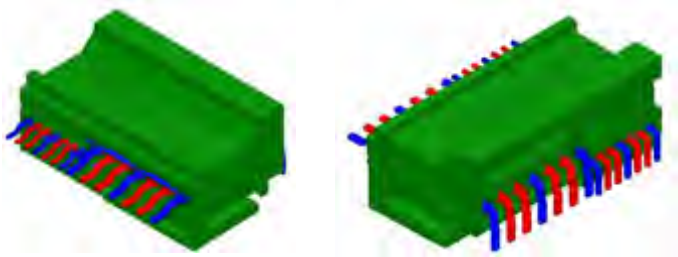
- **SAS-3 plug**
  - 2.5” Right angle surface mount plug
  - Molex S/#: 78695
- **SAS-3 receptacle**
  - Standard vertical surface mount receptacle
  - Molex S/#: 78715

Designed Plug PCB



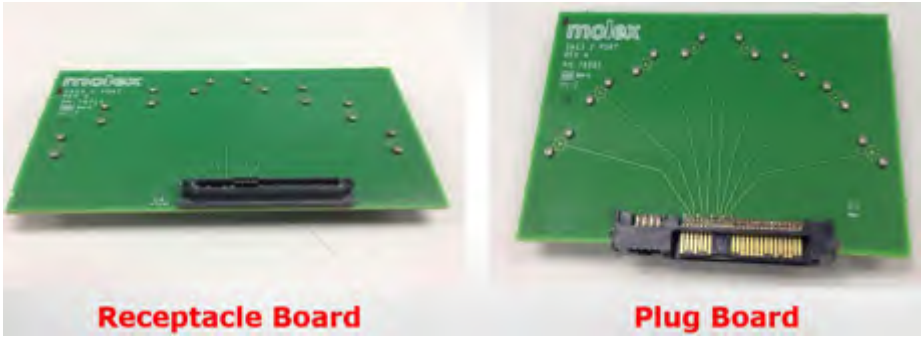
Designed Receptacle PCB





Connector Model

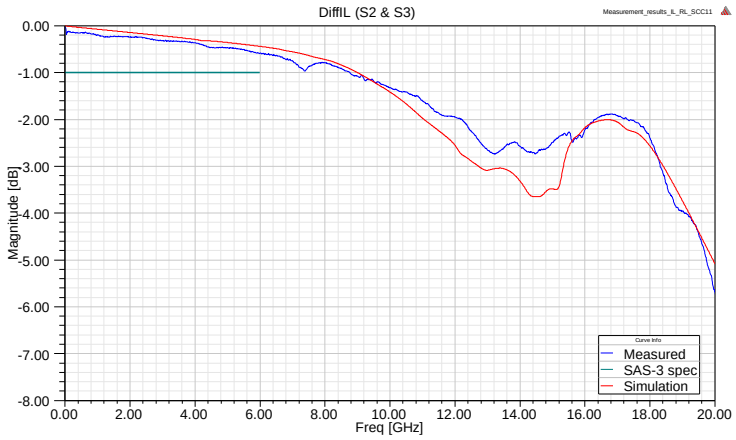
Test Fixtures



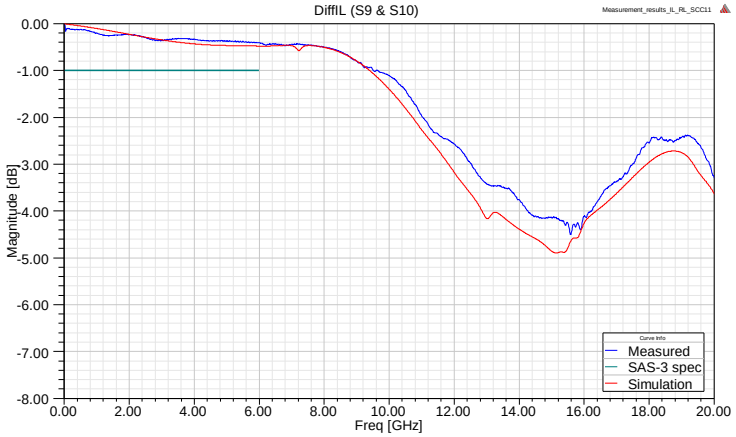
Differential S-Parameter Correlation Results

Insertion Loss

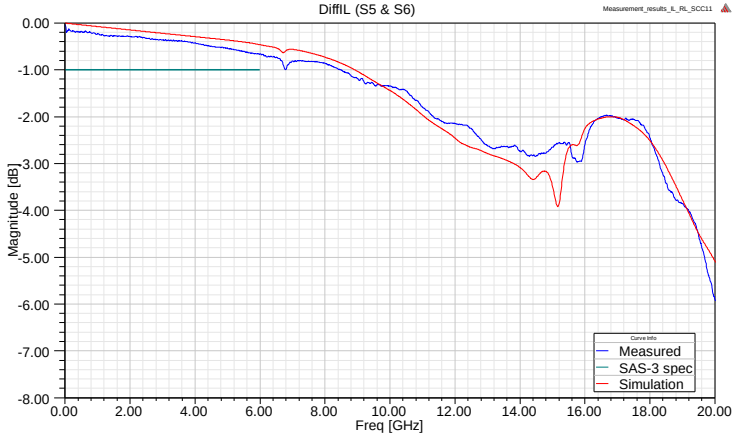
Port 1 pair 1 (S2 & S3)



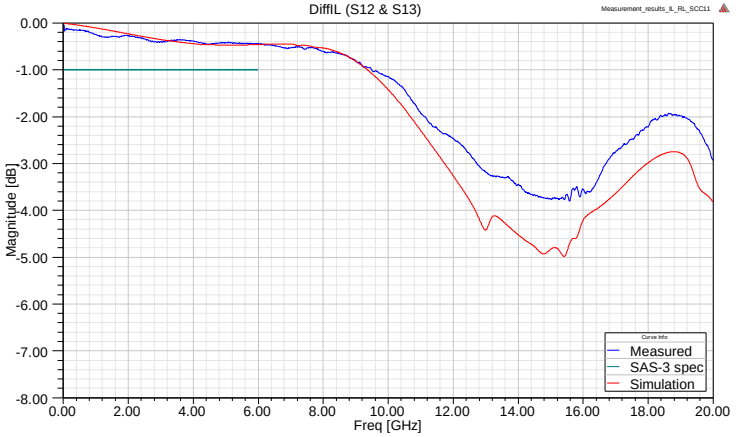
Port 2 pair 1 (S9 & S10)



Port 1 pair 2 (S5 & S6)

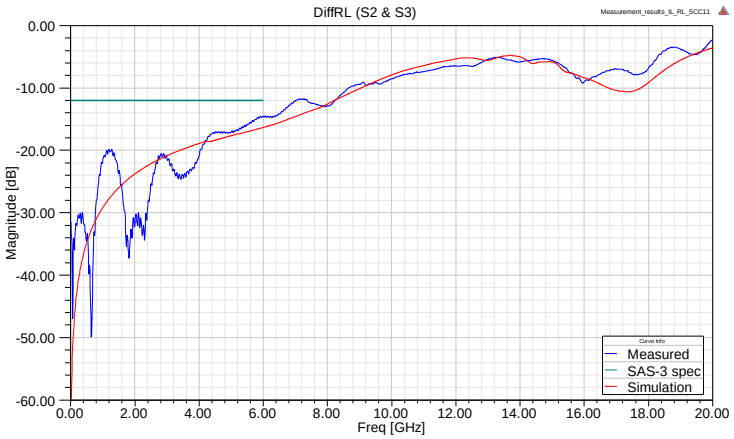


Port 2 pair 2 (S12 & S13)

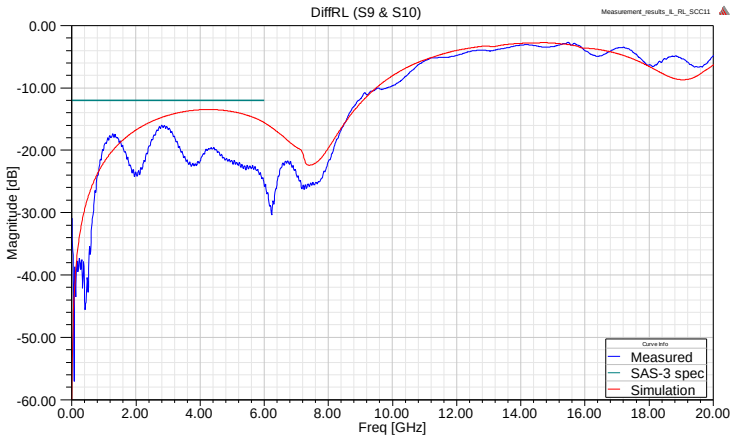


Return Loss

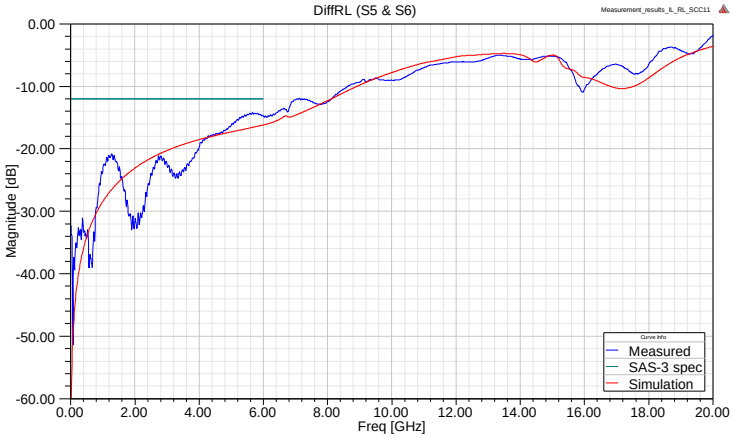
Port 1 pair 1 (S2 & S3)



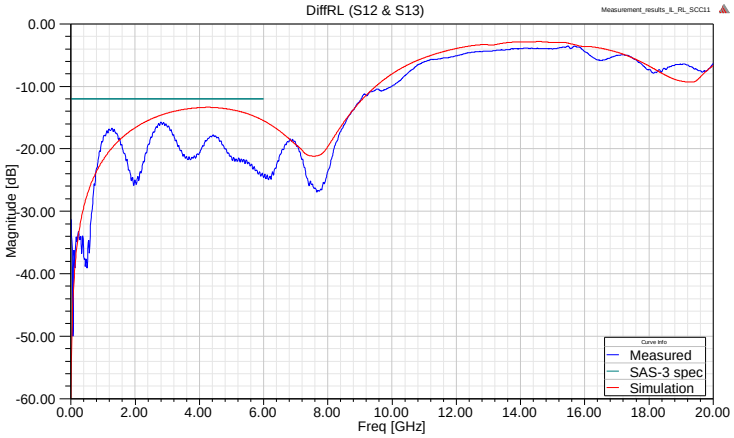
Port 2 pair 1 (S9 & S10)



Port 1 pair 2 (S5 & S6)

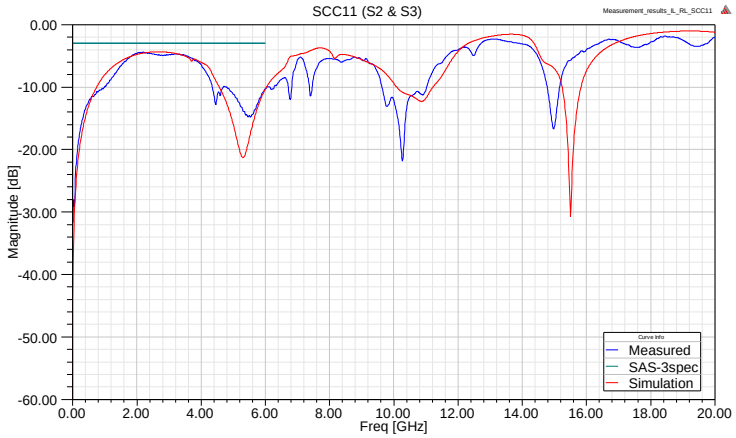


Port 2 pair 2 (S12 & S13)

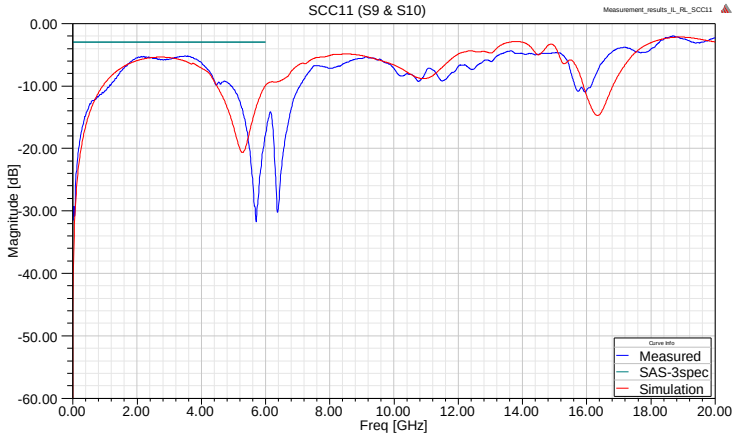


Common Mode

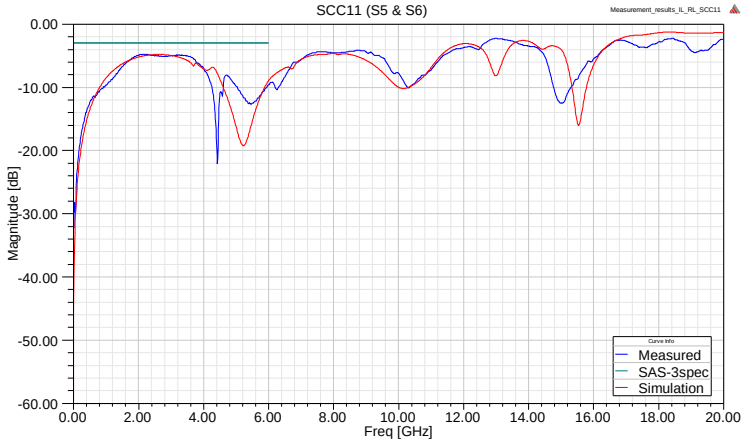
Port 1 pair 1 (S2 & S3)



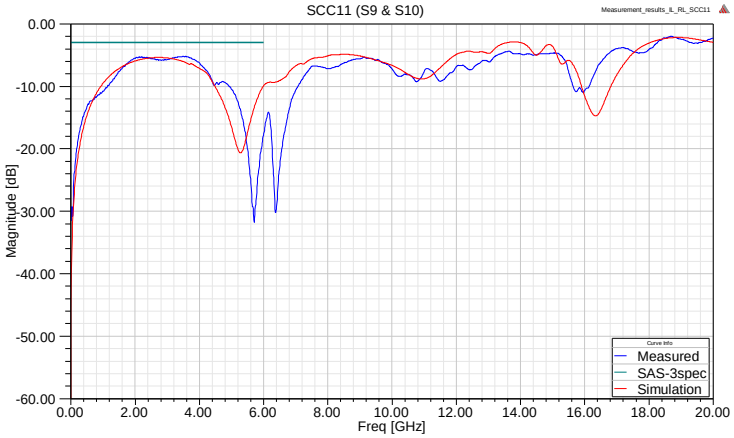
Port 2 pair 1 (S9 & S10)



Port 1 pair 2 (S5 & S6)

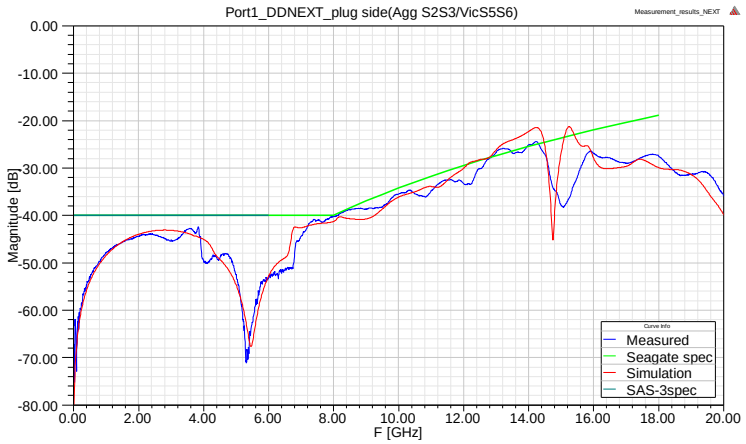


Port 2 pair 2 (S12 & S13)

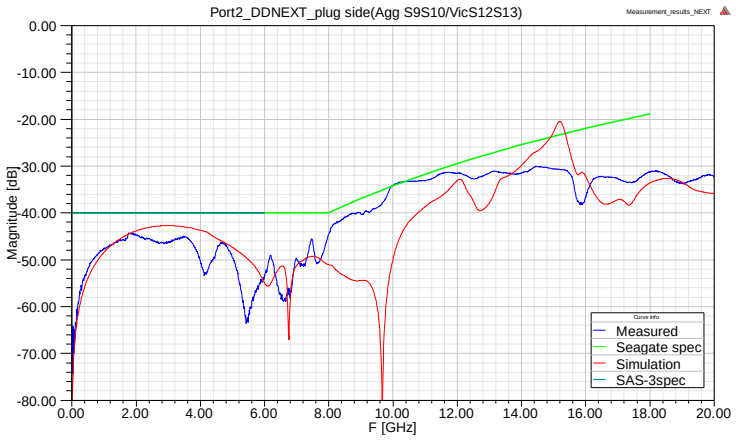


DDNEXT

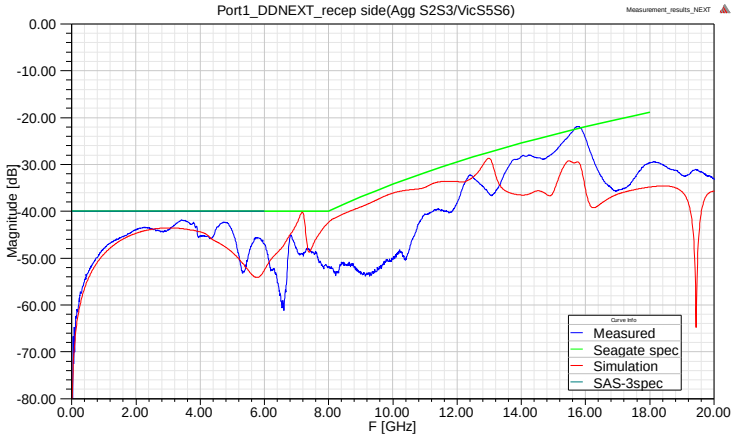
Port1pair1 Driven / Port1pair2 Victim (Plug side)



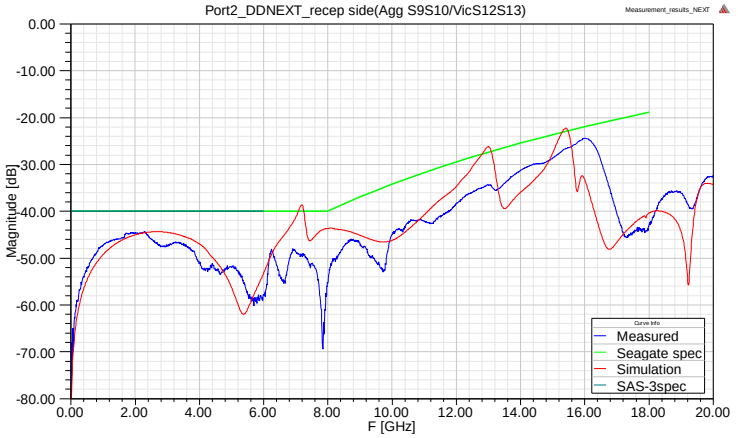
Port2pair1 Driven / Port2pair2 Victim (Plug side)



Port1pair1 Driven / Port1pair2 Victim (Receptacle side)

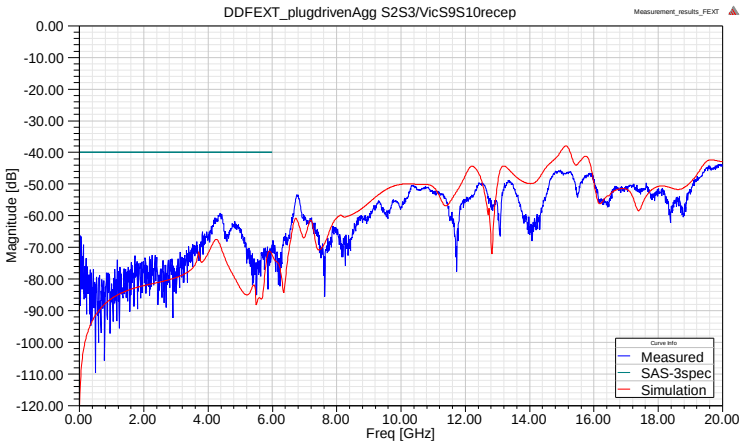


Port2pair1 Driven / Port2pair2 Victim (Receptacle side)

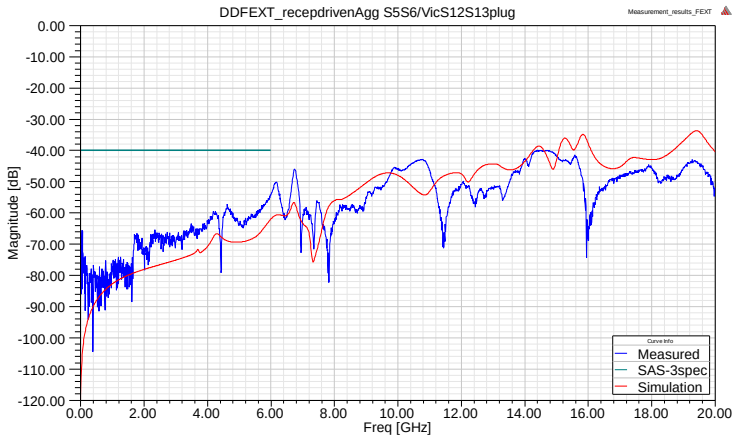


DDFEXT

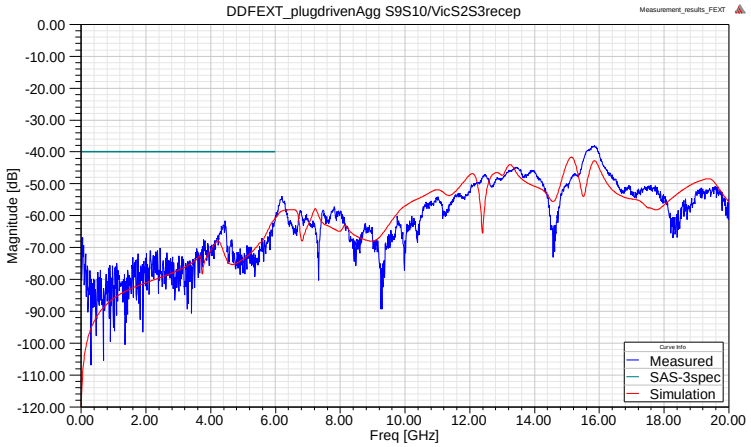
Port1pair1 Plug Side Driven / Port2pair1 Receptacle Side Victim



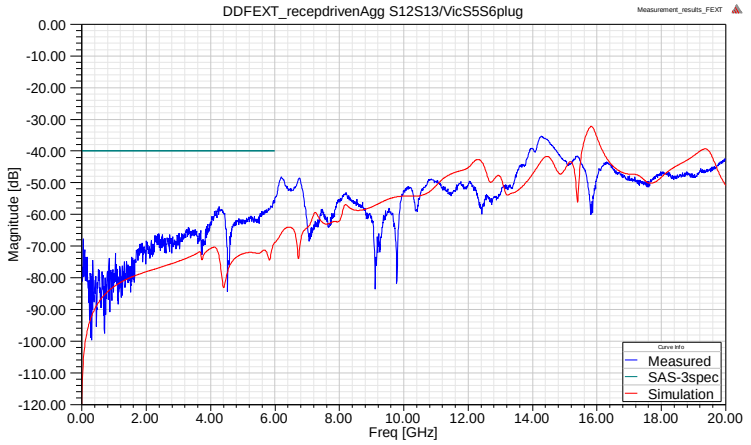
Port1pair2 Receptacle Side Driven / Port2pair2 Plug Side Victim



Port2pair1 Plug Side Driven / Port1pair1 Receptacle Side Victim



Port2pair2 Receptacle Side Driven / Port1pair2 Plug Side Victim

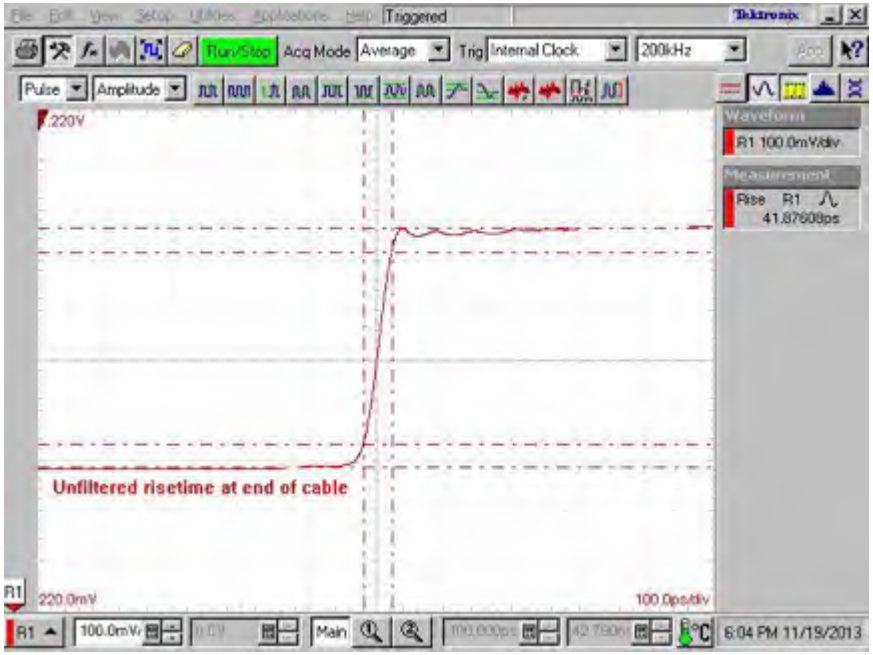


Observations

- The measured data correlated well with the simulated results with both sets of plots displaying similar shape and profile across the 20GHz bandwidth.
- The results had shown that the mated connector system will meet SAS-3 T10 requirements for SI.

Differential TDR Correlation Results

Differential TDR Risetime Definition

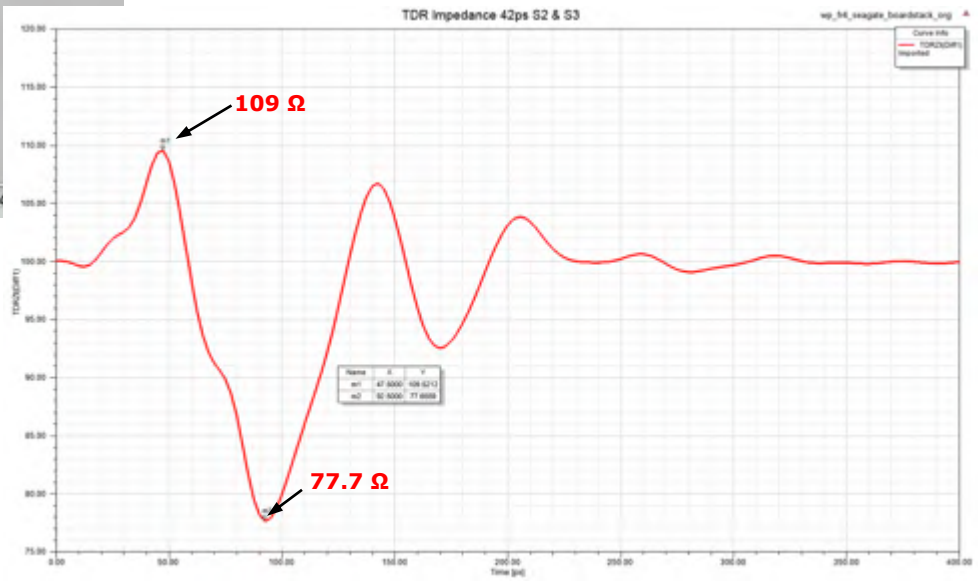


Risetime (10% - 90%) at end of 1m cable is approximately 42ps.

Measurement (from Tektronix)

TDR Plots @ 42ps (10% - 90%) – Port 1 pair 1 (S2 & S3)

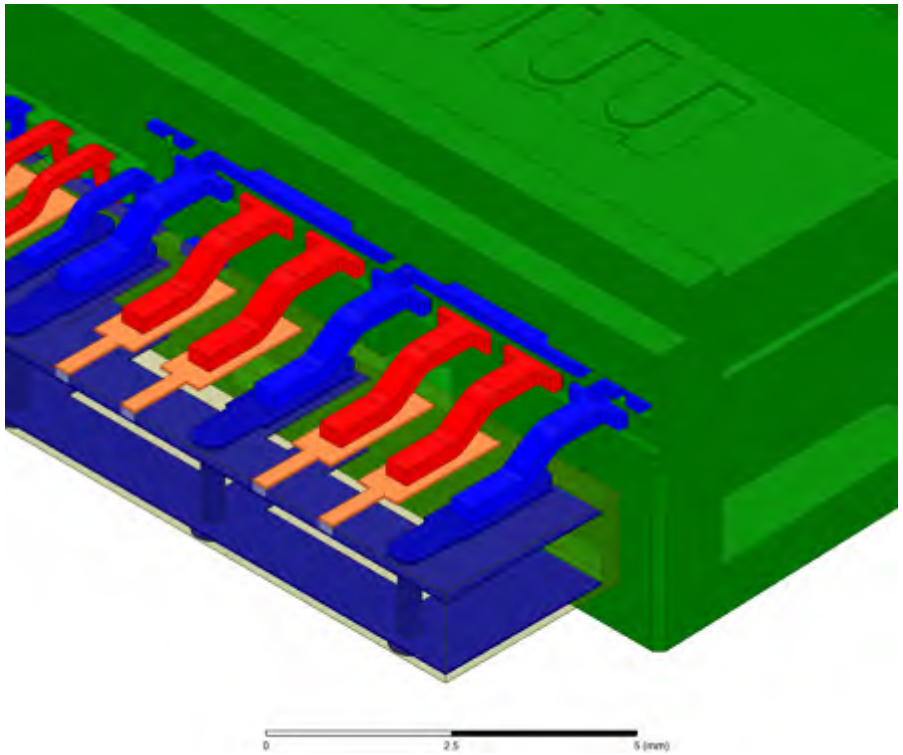
Simulation (from HFSS)



Accuracy:

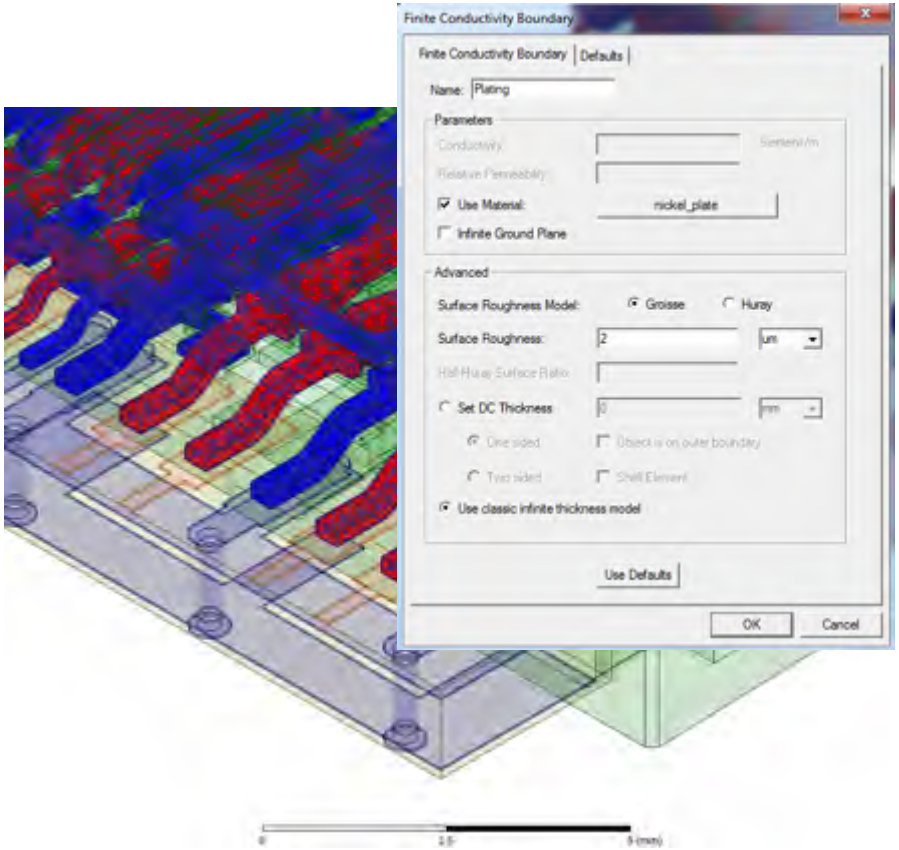
3% for high TDR and 12% for low TDR.

Model Comparison



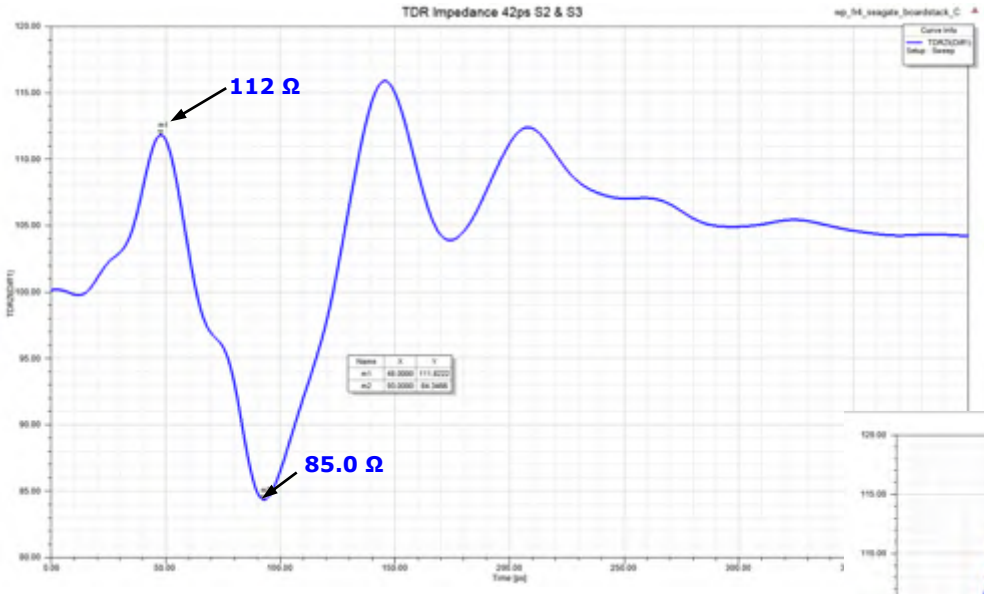
Original Model

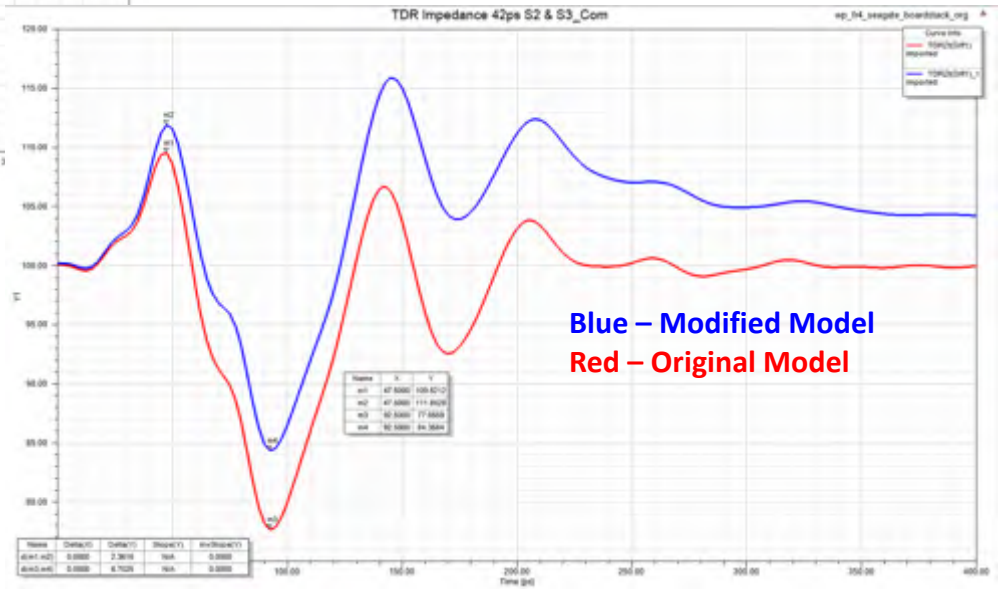
Add Nickel as a Finite Conductivity Boundary on Connector pins surface



Modified Model

Modified Model



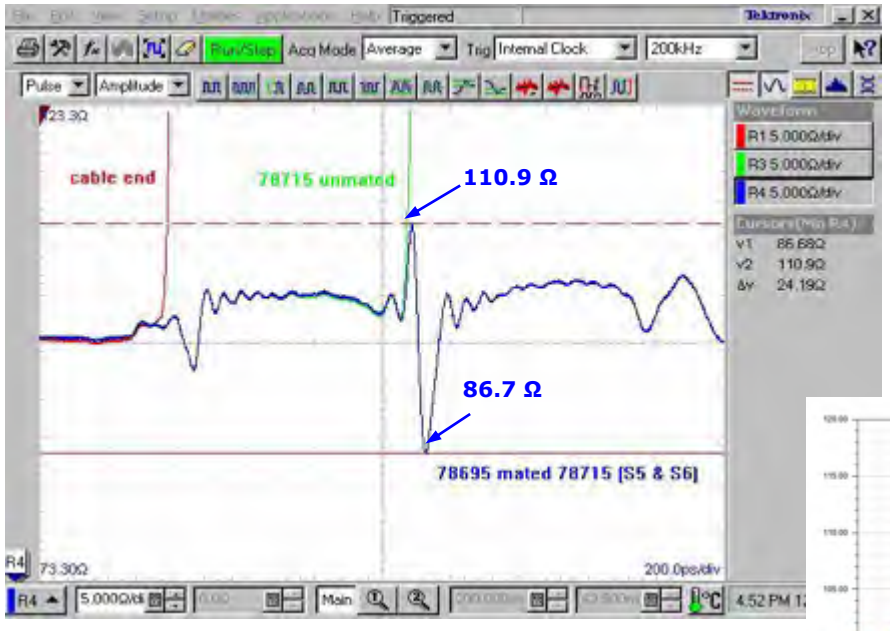


Accuracy

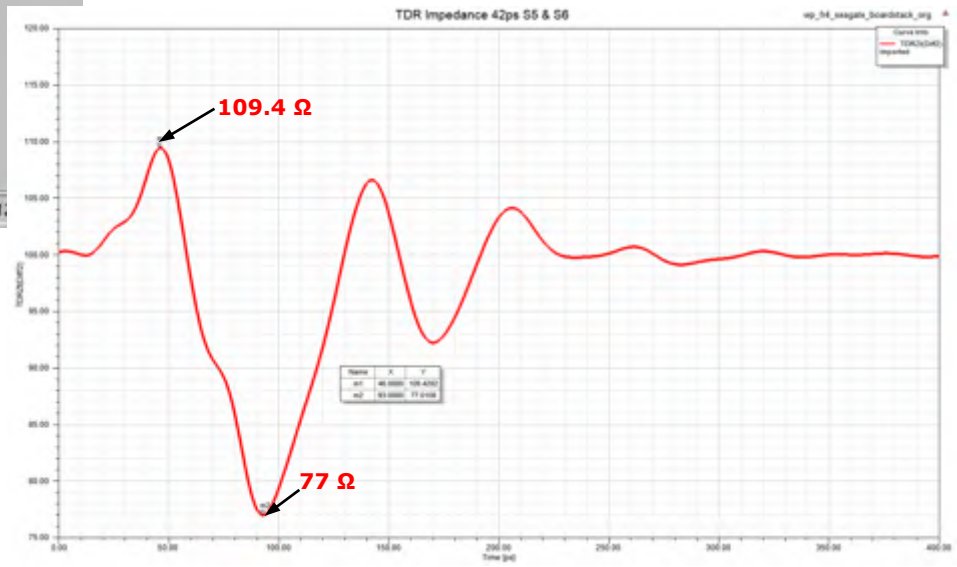
0.4% for high TDR and 3.4% for low TDR.

Measurement (from Tektronix)

TDR Plots @ 42ps (10% - 90%) – Port 1 pair 2 (S5 & S6)



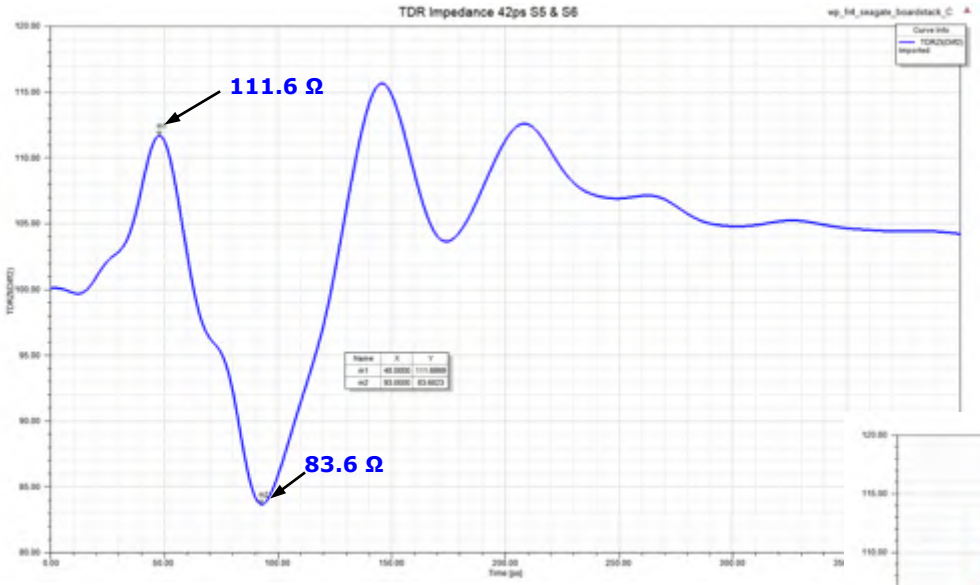
Simulation (from HFSS)

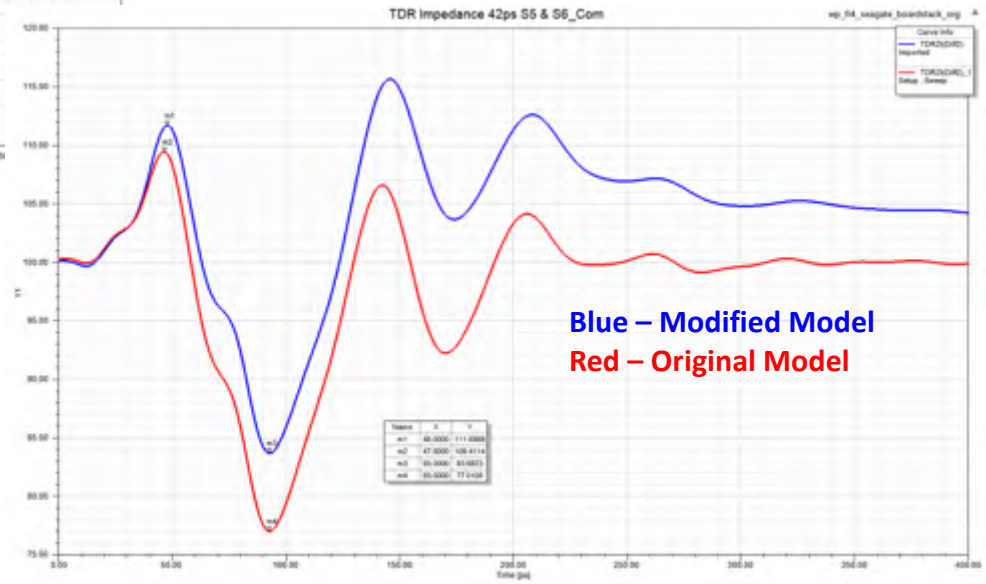


Accuracy:

1.35% for high TDR and 11% for low TDR.

Modified Model



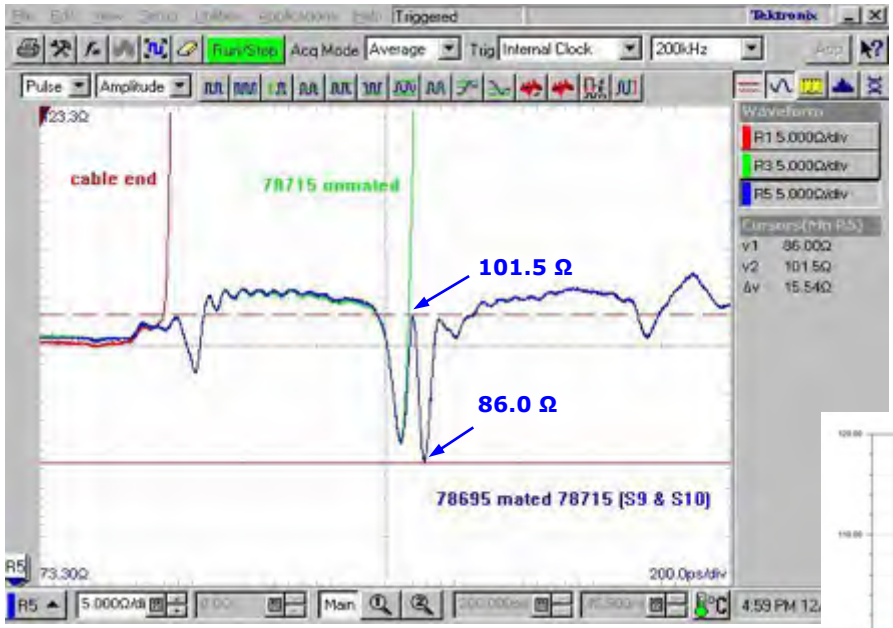


Accuracy

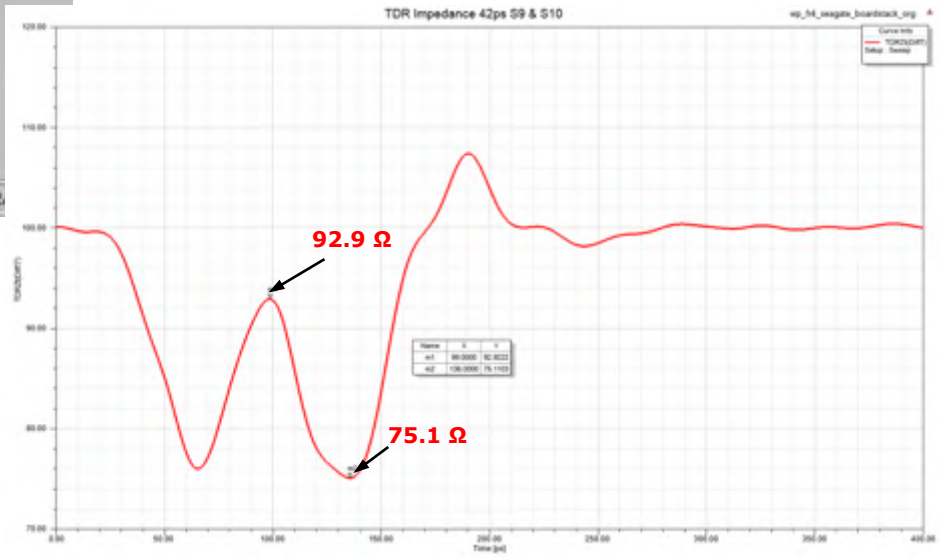
0.63% for high TDR and 3.57% for low TDR.

Measurement (from Tektronix)

TDR Plots @ 42ps (10% - 90%) – Port 2 pair 1 (S9 & S10)



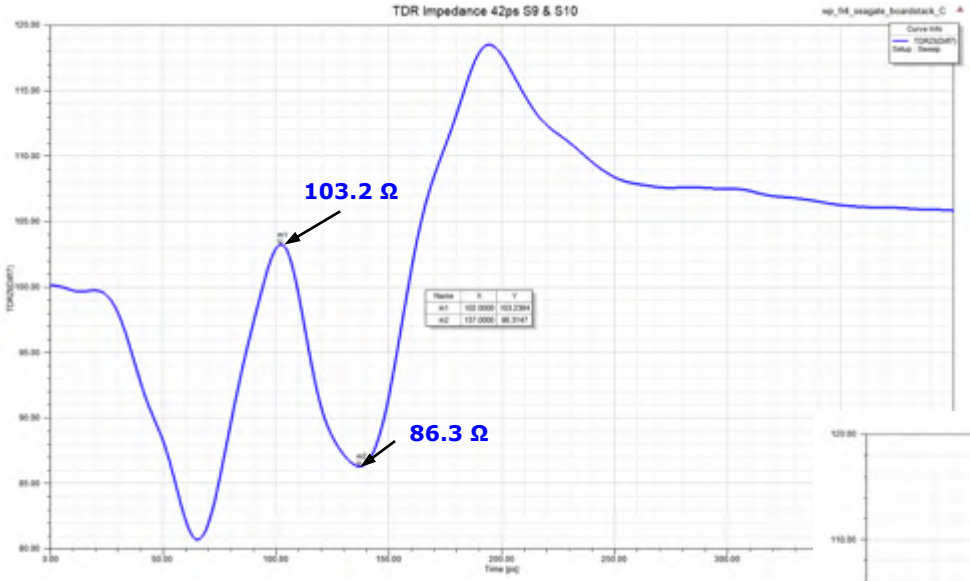
Simulation (from HFSS)

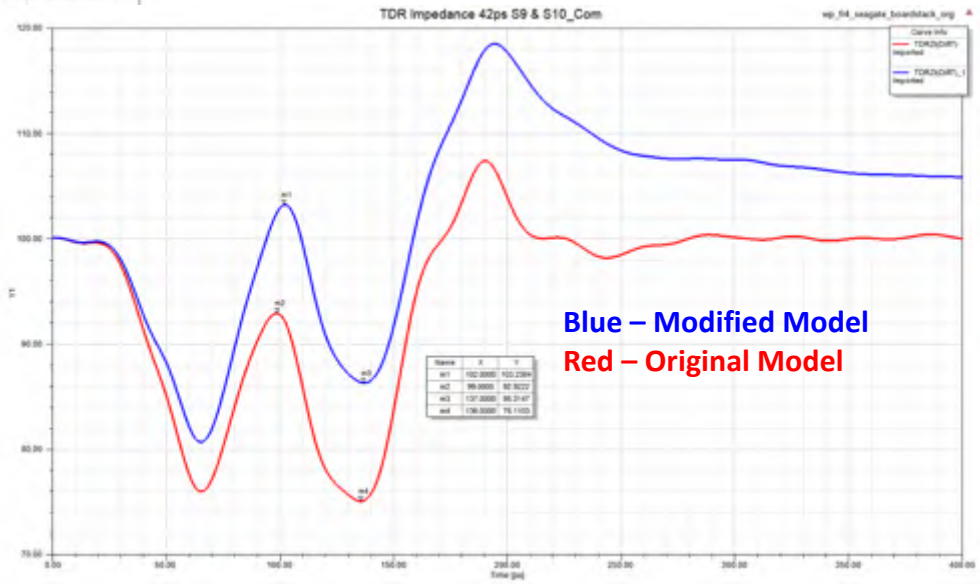


Accuracy:

8.4% for high TDR and 12.7% for low TDR.

Modified Model



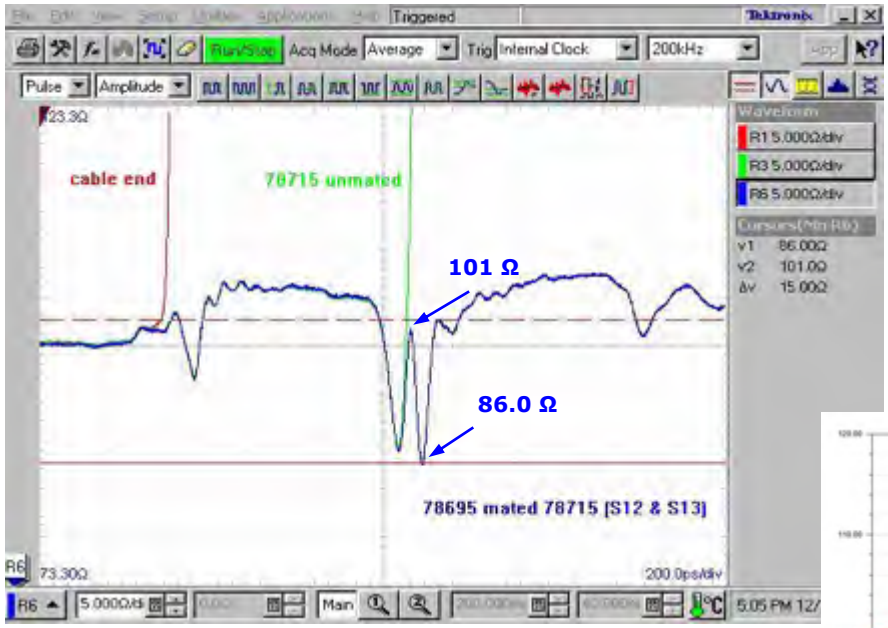


Accuracy

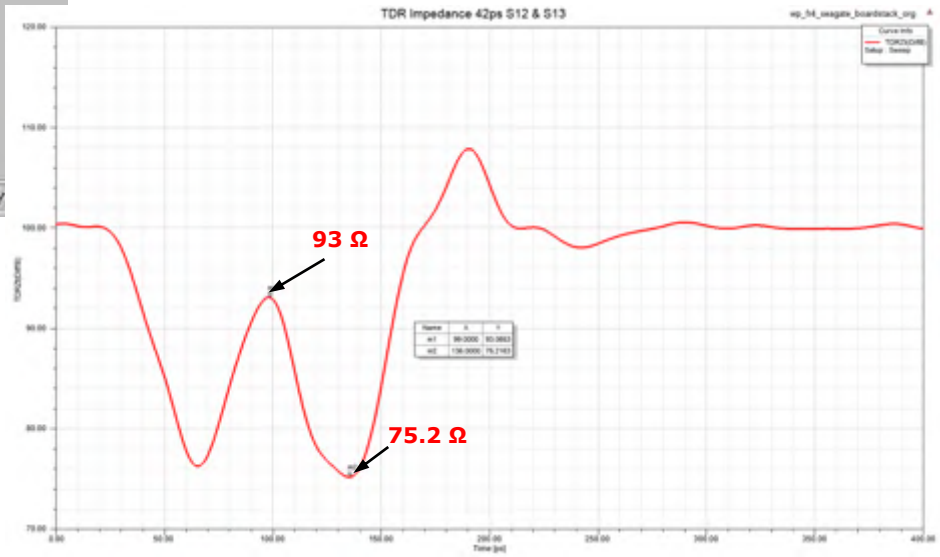
1.6% for high TDR and 0.35% for low TDR.

Measurement (from Tektronix)

TDR Plots @ 42ps (10% - 90%) – Port 2 pair 1 (S12 & S13)



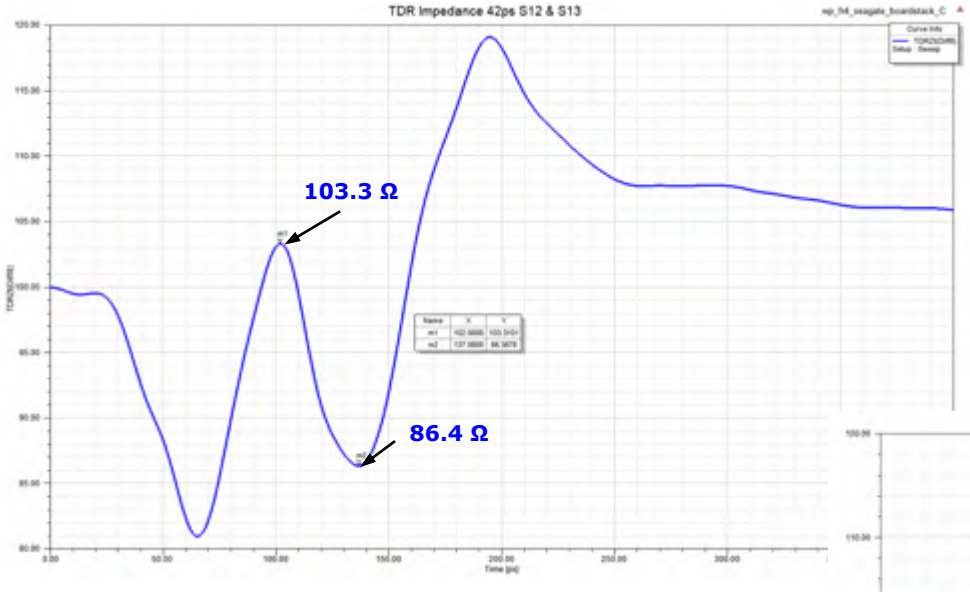
Simulation (from HFSS)

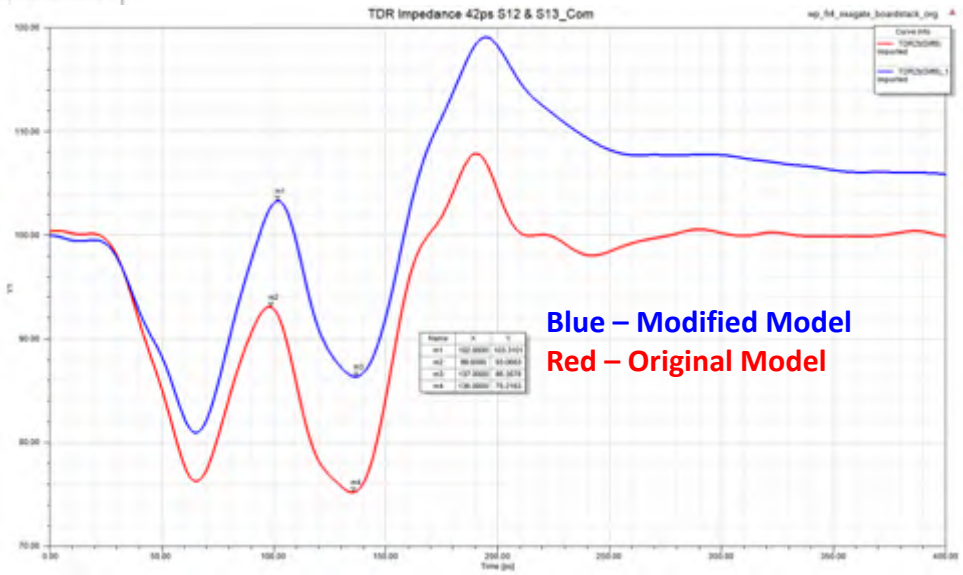


Accuracy:

7.9% for high TDR and 12.6% for low TDR.

Modified Model





Accuracy

2.2% for high TDR and 0.46% for low TDR.

Observations

- The measured Differential TDR correlated well with the simulated results with both sets of plots displaying similar shape and profile across the 400ps.
- The results had shown that the mated connector system will meet SAS-3 T10 requirements for TDR.

感谢聆听