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Thermal-aware SEB Methodology for Finfet design EM signoff

曾秋玲/ 工程师

海思半导体

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Statistical EM Budgeting(SEB) Introduction

- Historically designers have compared interconnect DC average current to a conservative fixed limit as,

  S = Jdesign / Jmax

- So if S <= 1, the “design” is reliable, while any interconnect with S > 1 needs to be redesigned. From the process reliability perspective, EM degradation is inherently statistical. There is always observed a wide dispersion in the times observed for identically sized and stressed segments of interconnect to progress to failure.

- When reliability design is designed to mean “achieving a chip-level reliability goal, fixed current density design limits become mathematically arbitrary. Only the total statistical risk to the chip is the meaningful. Then if the EM reliability impact of each segment of interconnect at each stress level can be accounted for, the chip-level EM reliability goal can be budgeted among classes of interconnect or chip design subdivisions to minimize the performance limitations.

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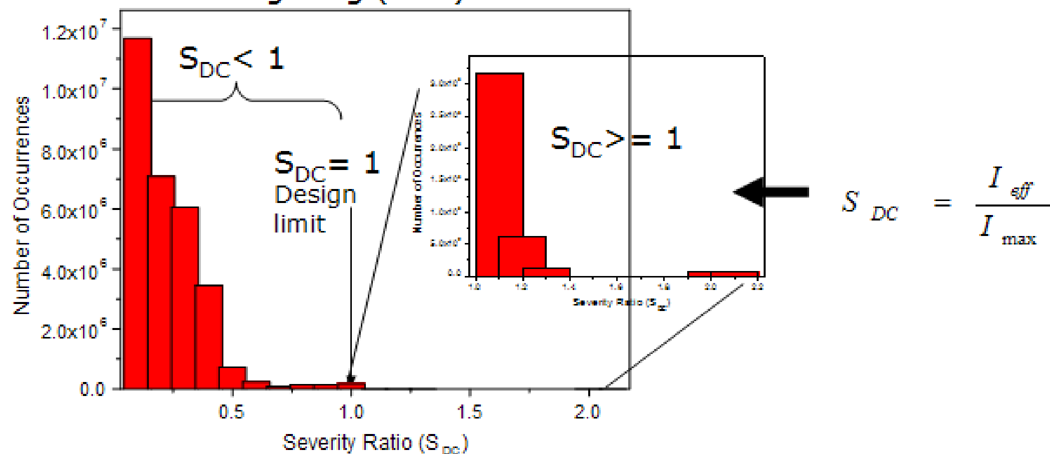
SEB Methodology

- Statistical EM Budgeting (SEB) is a design-specific EM reliability evaluation method which combines design inputs with EM performance for each interconnect wire to compute a total failure rate for the product. A “pass” is ascertained if the design stay within the failure budget.



$$S_{DC} = \frac{I_{eff}}{I_{max}}$$

- SEB gives the designers some flexibility in design without imposing a hard EM limit for the whole product, thus enabling higher performance without compromising reliability.

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Failure in Time (FIT) Calculation per Wire

$$FIT_i = \frac{(-10)^9}{LT} * \ln\left(1 - \Phi\left(\frac{\ln(S_{DC}^n *(LT/MTF))}{\sigma}\right)\right)$$

- LT = lifetime eg 5 or 10 years.
- Φ = std normal cumulative distribution probability
- Sdc = severity ratio of Idc, I/Imax:

  I-> from design,

  Imax-> defined in design rule manual.
- n = current density exponent (from foundry)
- MTF = median time to failure

  MTF(Tfit)=MTF(Tamb) * exp(Ea/Kb *(1/(Tfit+273)-1/(Tamb+273)))

  Tamb=Ambient Temperature; Tfit=Tamb+ ΔT from self-heating
- σ = sigma, spread in lifetime distribution (from foundry)

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Why SEB

- **EM challenge on advanced FinFet process**
  - EM is significantly impact on FEOL thermal coupling and self-heating
  - Very difficult to sign-off EM due to EM limit degraded significantly.

- **Life Time**
  - EM spec definition in DRM are based on 10Y life time. How about 5Y life time?
  - Real application: 5% x Life time 125c + 95% x Life time 85c

- **From one net to a design**
  - If every net satisfy EM spec, the design have high reliability? NO!

    For example：

    Condition: TSMC N10, 10Y life time

    Sdc（I/Imax)=0.8, fail rate =0.15%(1500PPM). If there are many nets with Sdc more than 0.8, the total fail rate is more high.

    Usually, SOC fail rate < 0.1%

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FIT calculation

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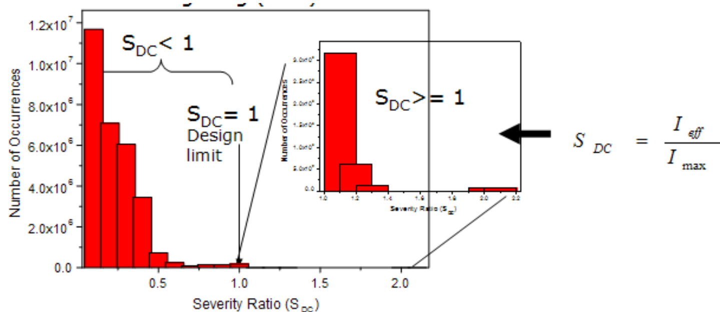

$$S_{DC} = \frac{I_{eff}}{I_{max}}$$

$$FIT_{total} = \sum^{i} \sum^{j} \sum^{k} FIT(i,j,k)$$

Sub-divisions classes wires

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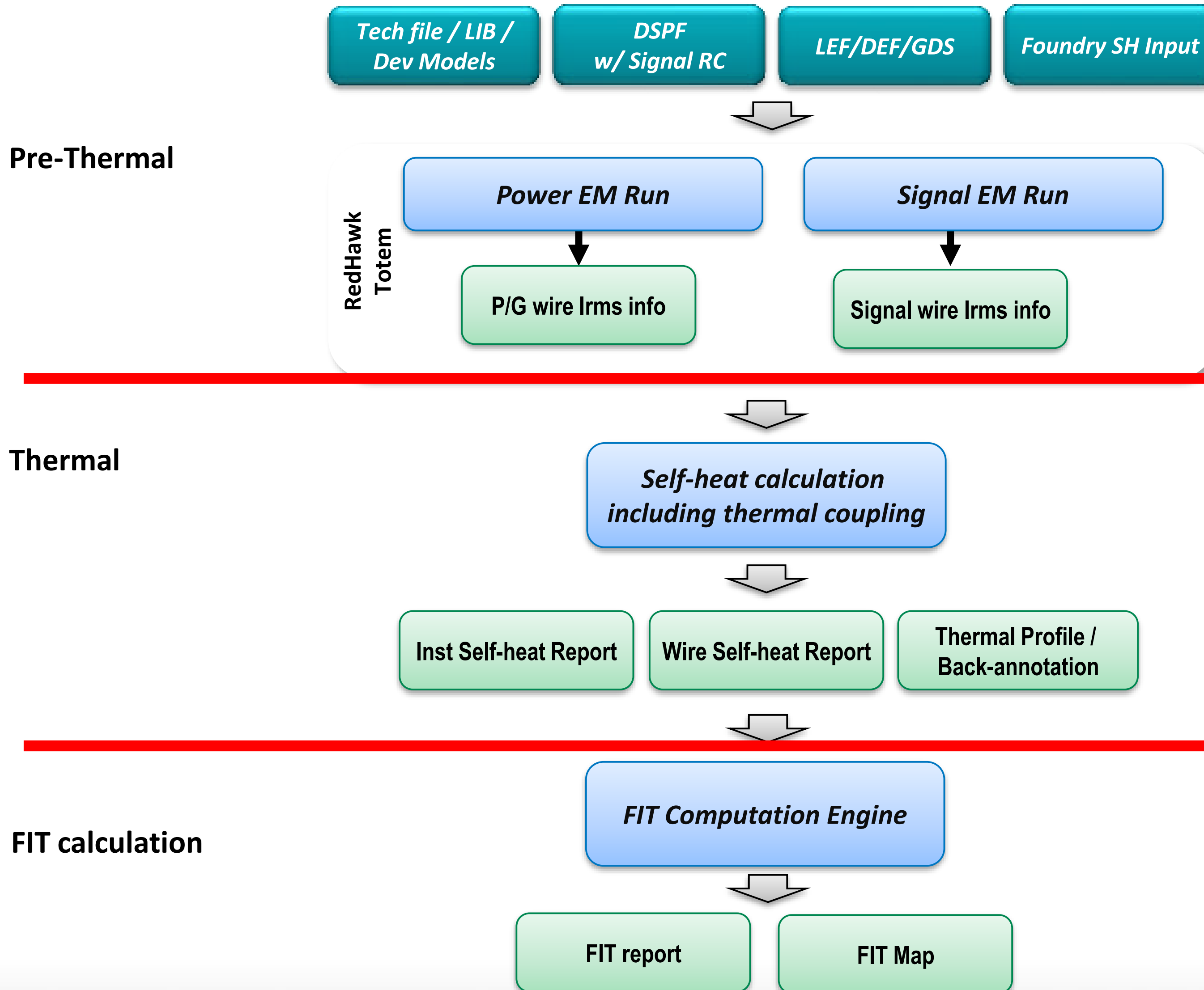
Thermal-Aware SEB Flow



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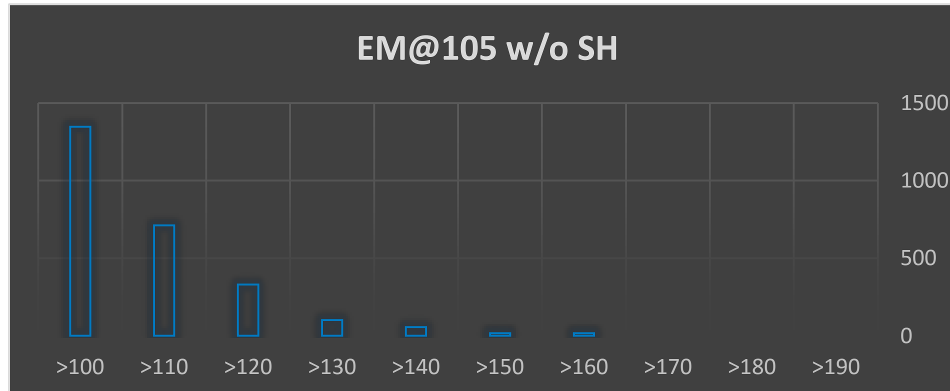
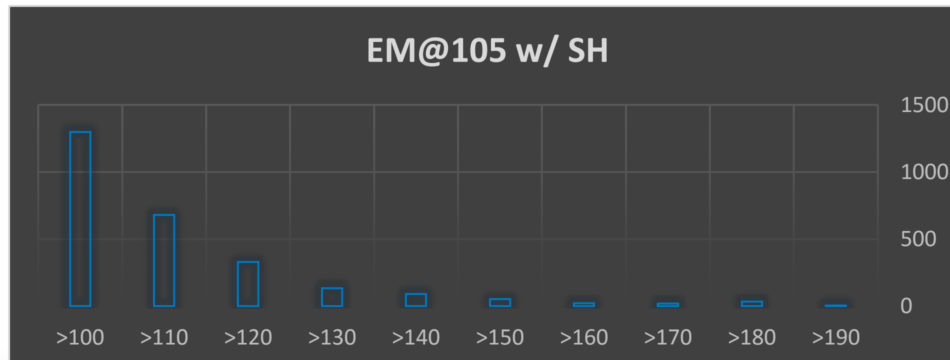
Self-heating impact on EM

	@105C w/o Self-heating	@105 w/ Self-heating
Number of EM violations	2581	2664
Max EM violation	168%	197%
Total FIT	23	416





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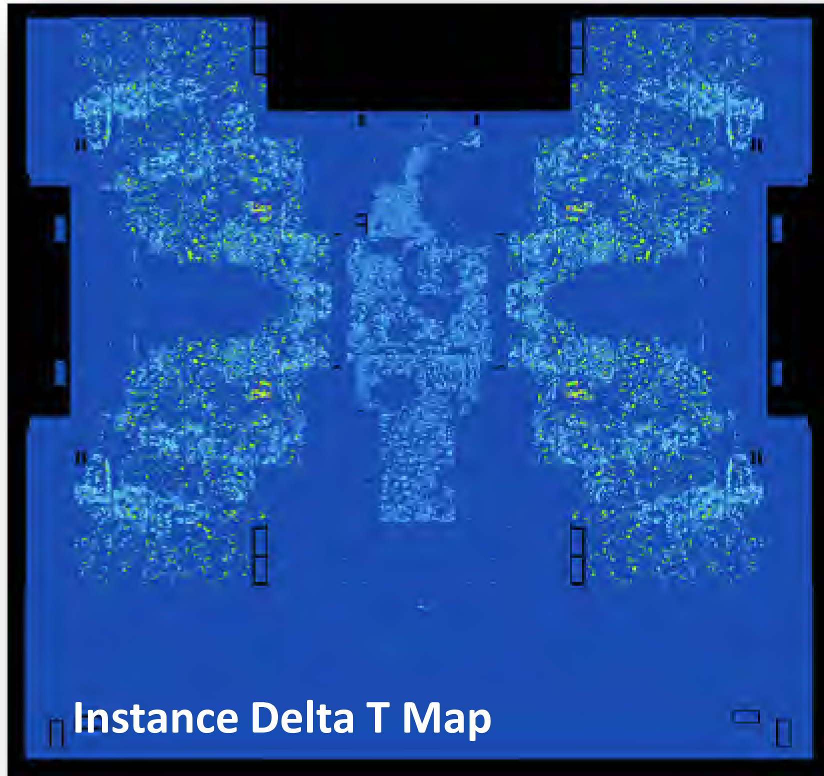
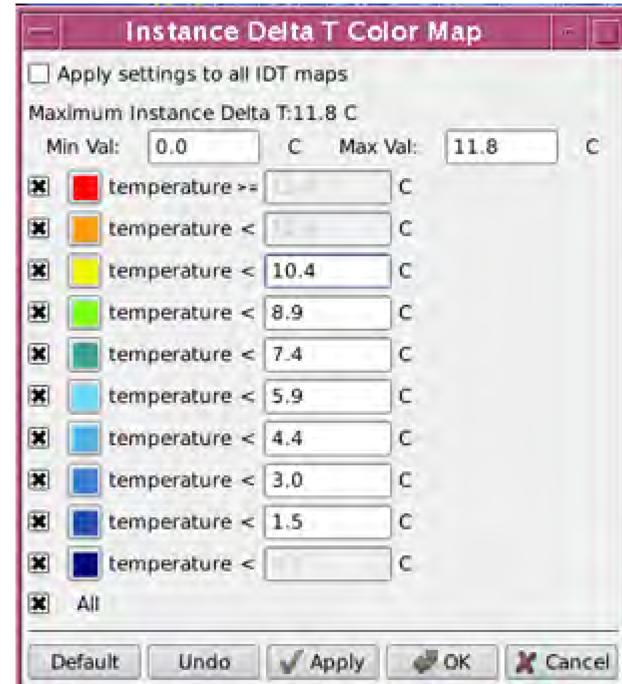
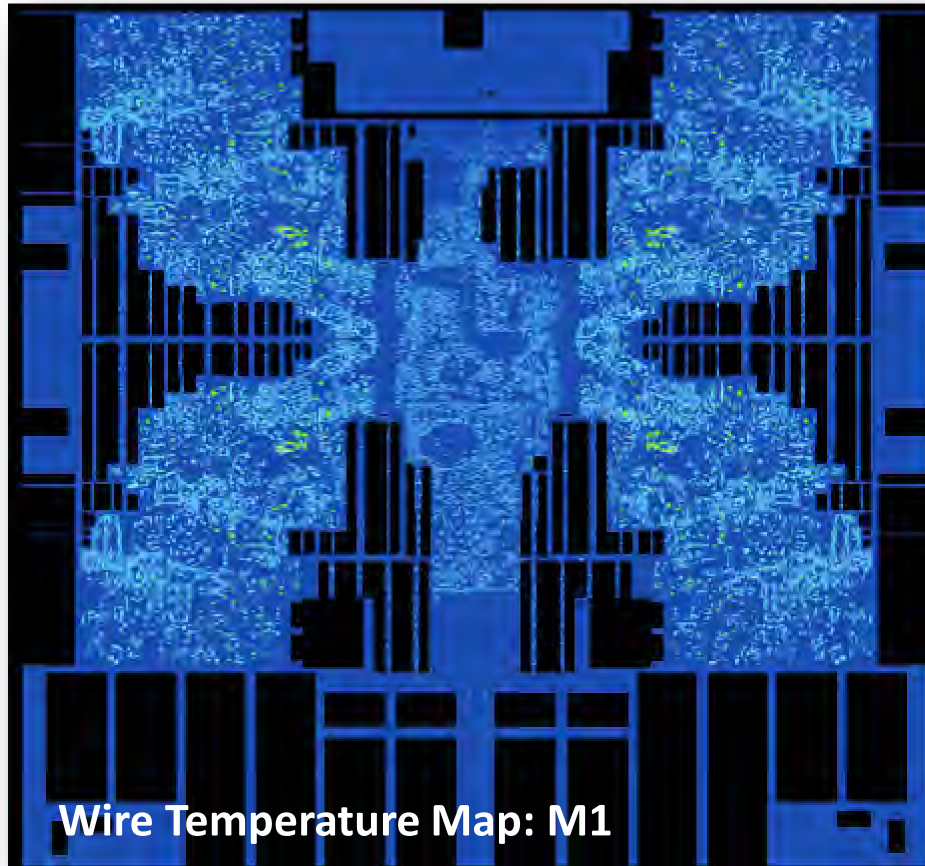
Self-heating Result: instance delta T





The max delta T is 11.8C

Wire Temperature: Max temperature 116.5C



Wire Temperature Color Map

☐ Apply settings to all WT maps

Temperature Low: 105 Temperature High: 116.462

Min. Value: 105 Max. Value: 115

	Color	Condition	Value
☒	red	temperature >=	115.000
☒	orange	temperature <	115.000
☒	yellow	temperature <	113.750
☒	green	temperature <	112.500
☒	teal	temperature <	111.250
☒	light cyan	temperature <	110.000
☒	light blue	temperature <	108.750
☒	blue	temperature <	107.500
☒	dark blue	temperature <	106.250
☒	navy	temperature <	105.000
☒		All	

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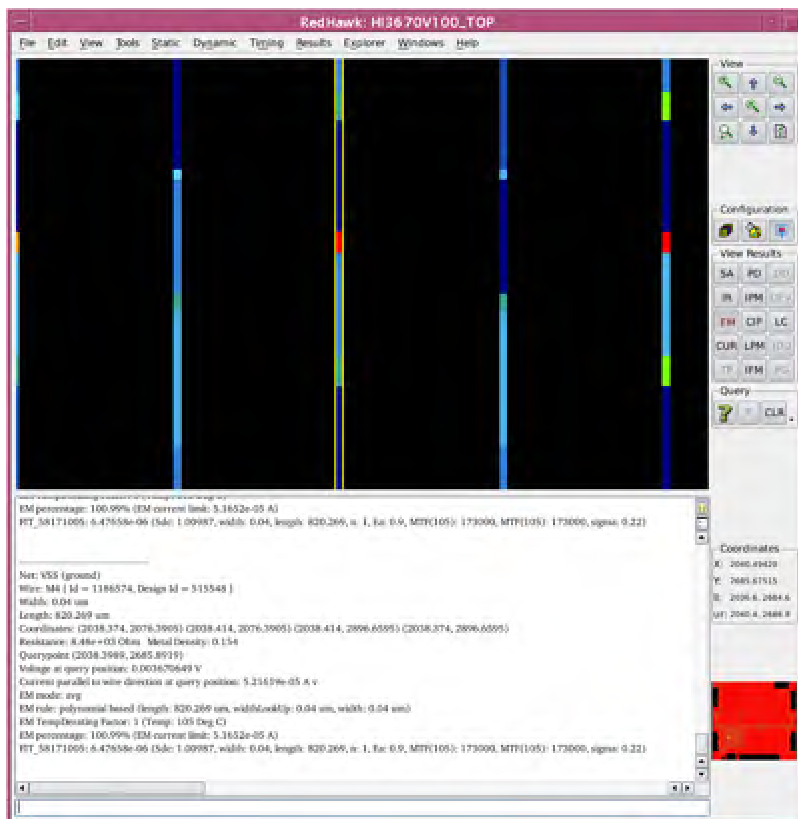
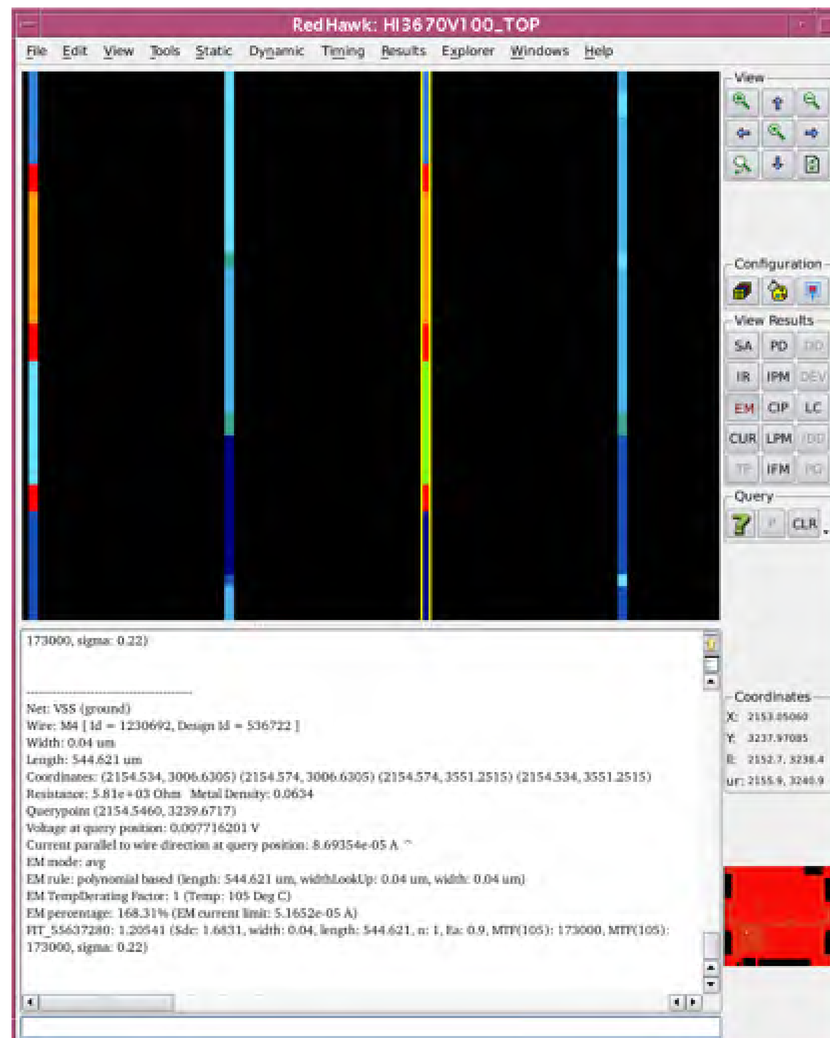
FIT correlation





use Year	use Hour	Sdc	temp	MTF	sigma	FIT	FIT in RedHawk	Error %
5	43800	1.01	105	1.73E+05	0.22	6.47613E-06	6.47658E-06	-0.00689%
5	43800	1.68	105	1.73E+05	0.22	1.20544E+00	1.20541E+00	0.00234%

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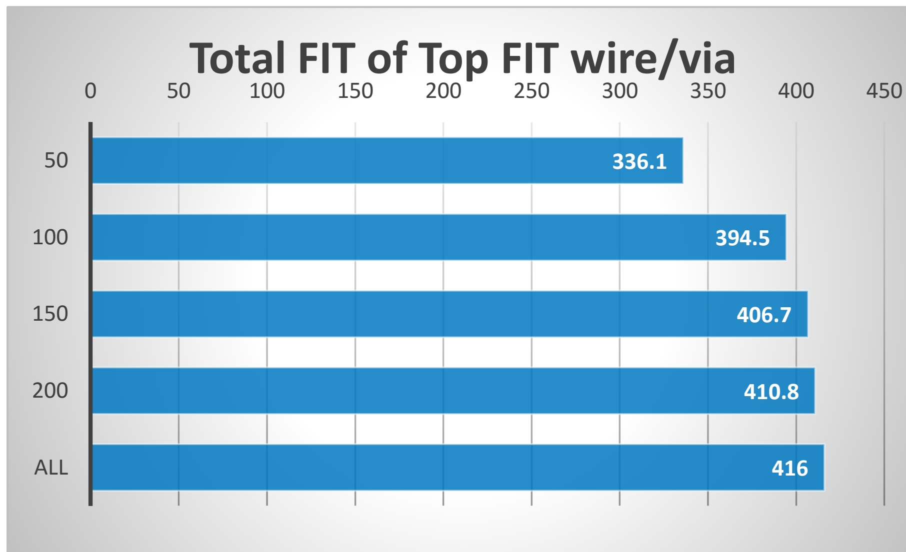
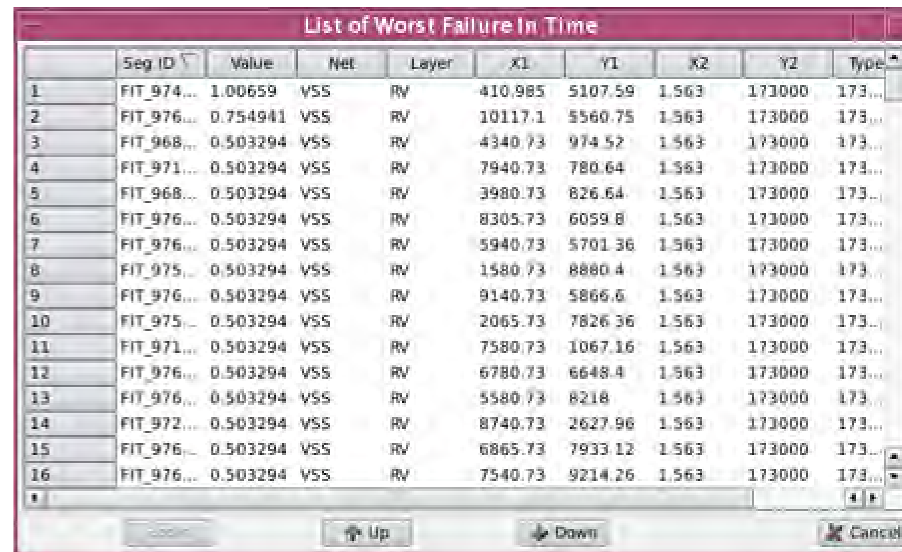
EM sign-off by thermal-aware SEB

- Designer should fix 2664 EM violations by traditional EM sign-off method.
- Now design can be sign-off if fix less than 200 violations.




List of Worst Failure In Time

	Seg ID	Value	Net	Layer	X1	Y1	X2	Y2	Type
1	FIT_974...	1.00659	VSS	RV	410.985	5107.59	1.563	173000	173...
2	FIT_976...	0.754941	VSS	RV	10117.1	5560.75	1.563	173000	173...
3	FIT_968...	0.503294	VSS	RV	4340.73	974.52	1.563	173000	173...
4	FIT_971...	0.503294	VSS	RV	7940.73	780.64	1.563	173000	173...
5	FIT_968...	0.503294	VSS	RV	3980.73	826.64	1.563	173000	173...
6	FIT_976...	0.503294	VSS	RV	8305.73	6059.8	1.563	173000	173...
7	FIT_976...	0.503294	VSS	RV	5940.73	5701.36	1.563	173000	173...
8	FIT_975...	0.503294	VSS	RV	1580.73	8880.4	1.563	173000	173...
9	FIT_976...	0.503294	VSS	RV	9140.73	5866.6	1.563	173000	173...
10	FIT_975...	0.503294	VSS	RV	2065.73	7826.36	1.563	173000	173...
11	FIT_971...	0.503294	VSS	RV	7580.73	1067.16	1.563	173000	173...
12	FIT_976...	0.503294	VSS	RV	6780.73	6648.4	1.563	173000	173...
13	FIT_976...	0.503294	VSS	RV	5580.73	8218	1.563	173000	173...
14	FIT_972...	0.503294	VSS	RV	8740.73	2627.96	1.563	173000	173...
15	FIT_976...	0.503294	VSS	RV	6865.73	7933.12	1.563	173000	173...
16	FIT_976...	0.503294	VSS	RV	7540.73	9214.26	1.563	173000	173...

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