Bridging among Chip, Package And System in the Industry

Youngsoo Lee

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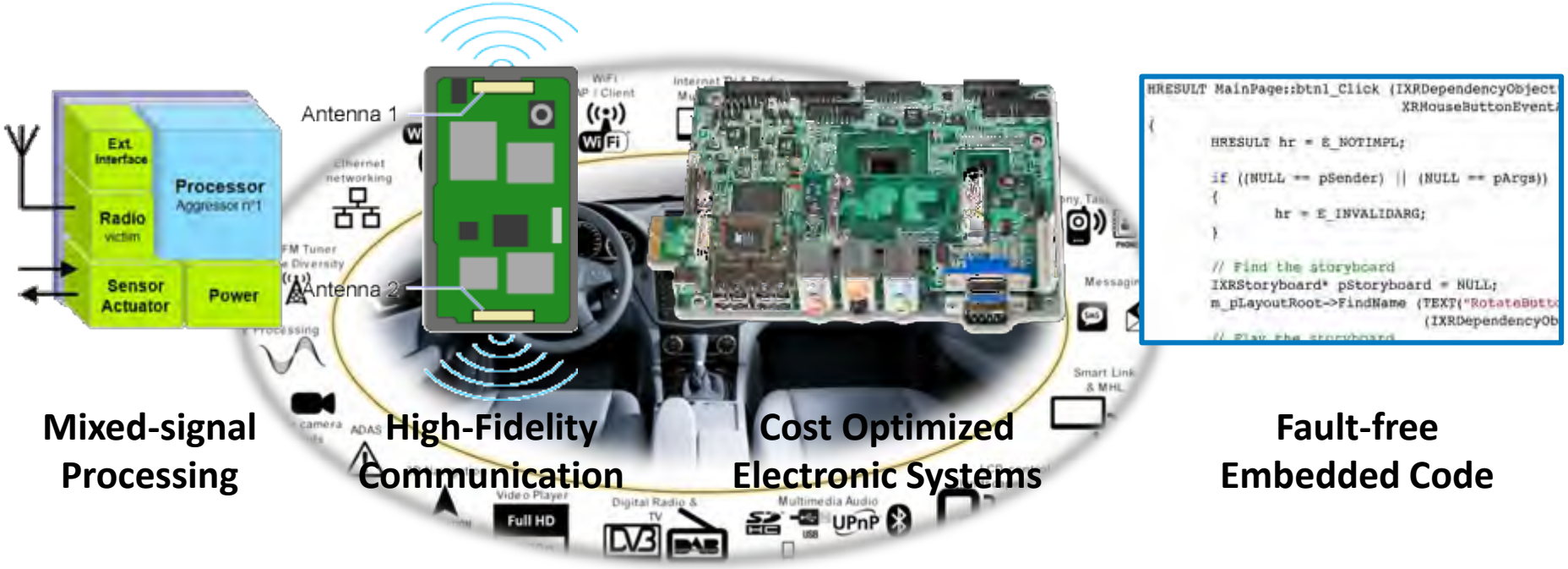
ANSYS

Electronic System Design Challenges



Mixed-signal Processing

High-Fidelity Communication

Cost Optimized Electronic Systems

Fault-free Embedded Code

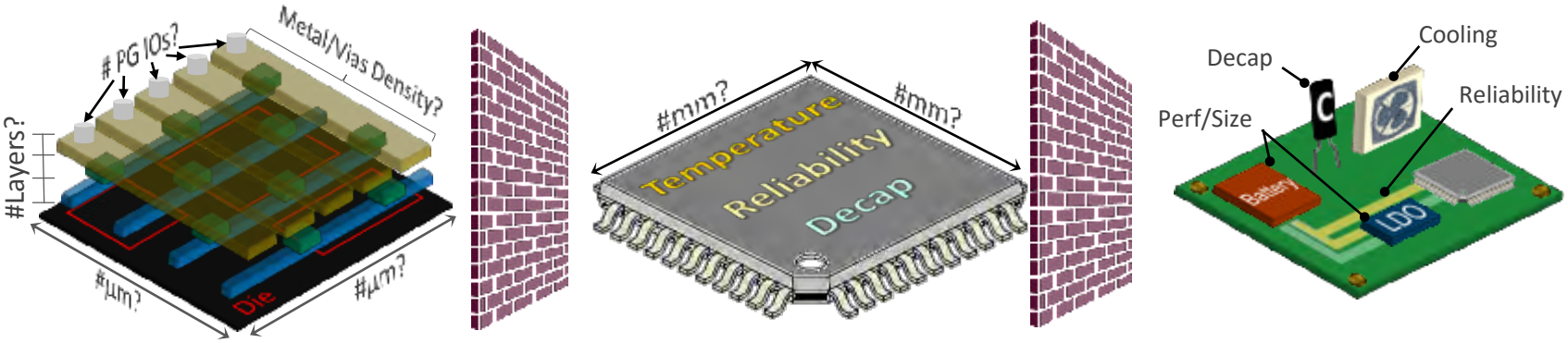
Low Power

Cost Reduction

Complexity Management

Single-Platform Multiphysics and Multiscale Design Exploration Encompassing Entire Electronic System is Necessary

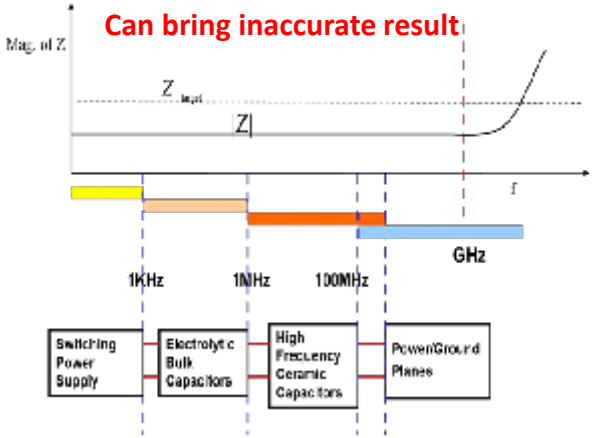
Industry Reality: Separated due to Conventional Env. & Silo



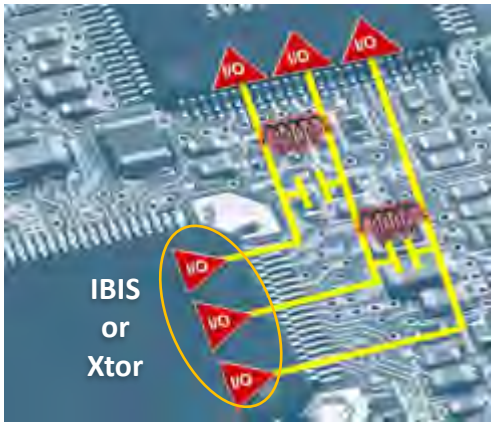
- Essential elements crucial to performance should be decided by co-design
- Separated chip, package and board development owner and process
- Insufficient information/interest about other parts due to silo
- No integrated team and design methodology encompassing all parts
- Different knowledge scope : alien to each other

Traditional Power/Signal/Thermal Performance Check

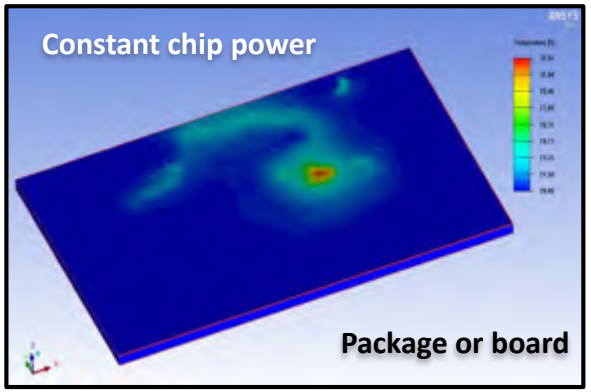
System Level: Individual part is designed with its own target spec



Power Integrity

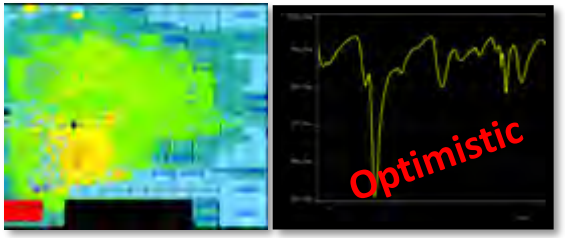


Signal Integrity

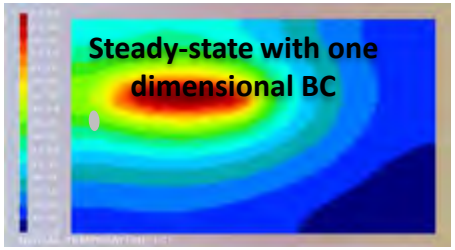


Thermal Integrity

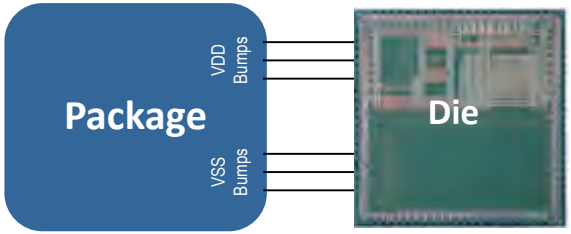
Chip Level: Chip only or lumped model, Manual Connection



Static & Dynamic IR drop w/o Package



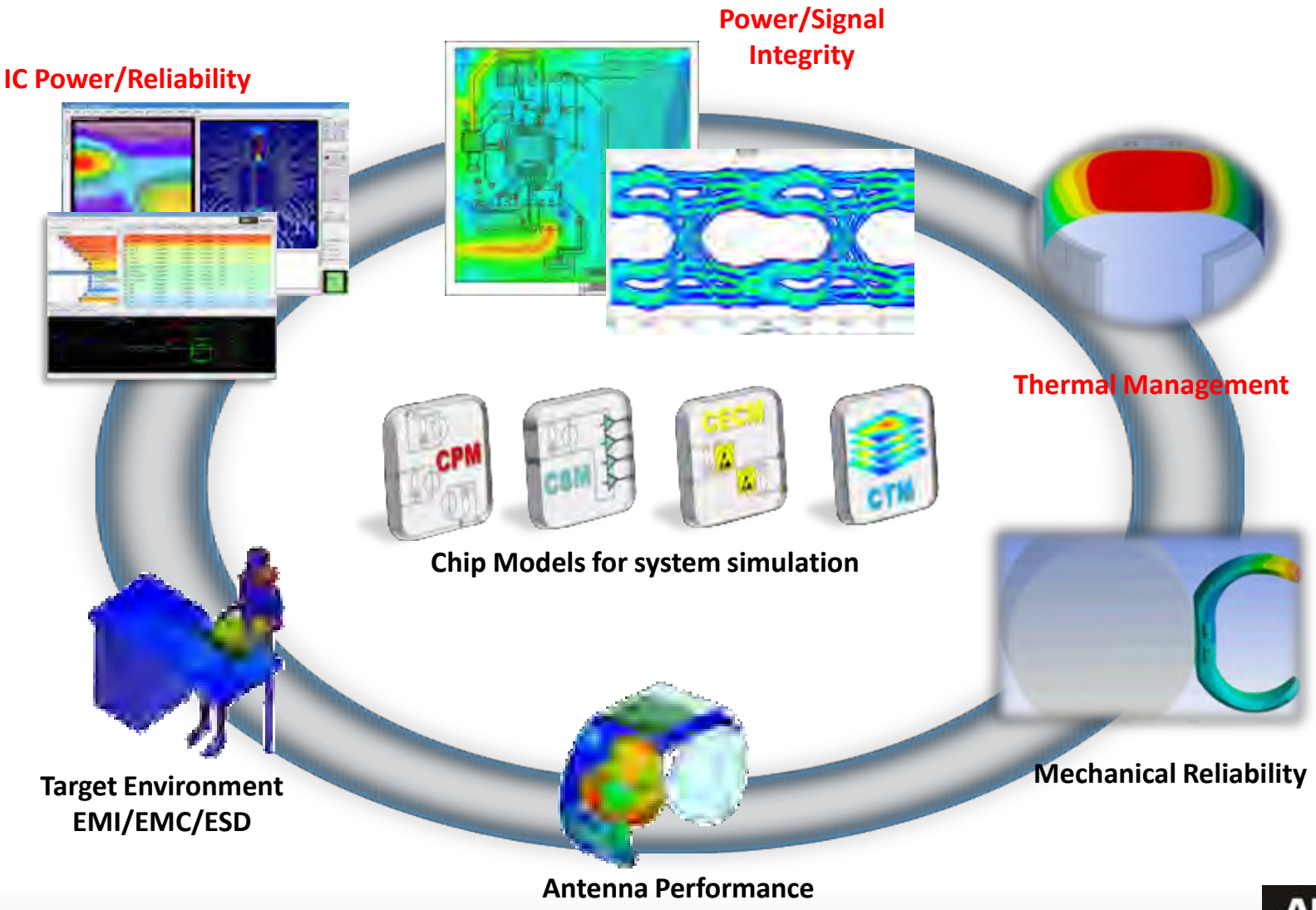
Chip Thermal Profile



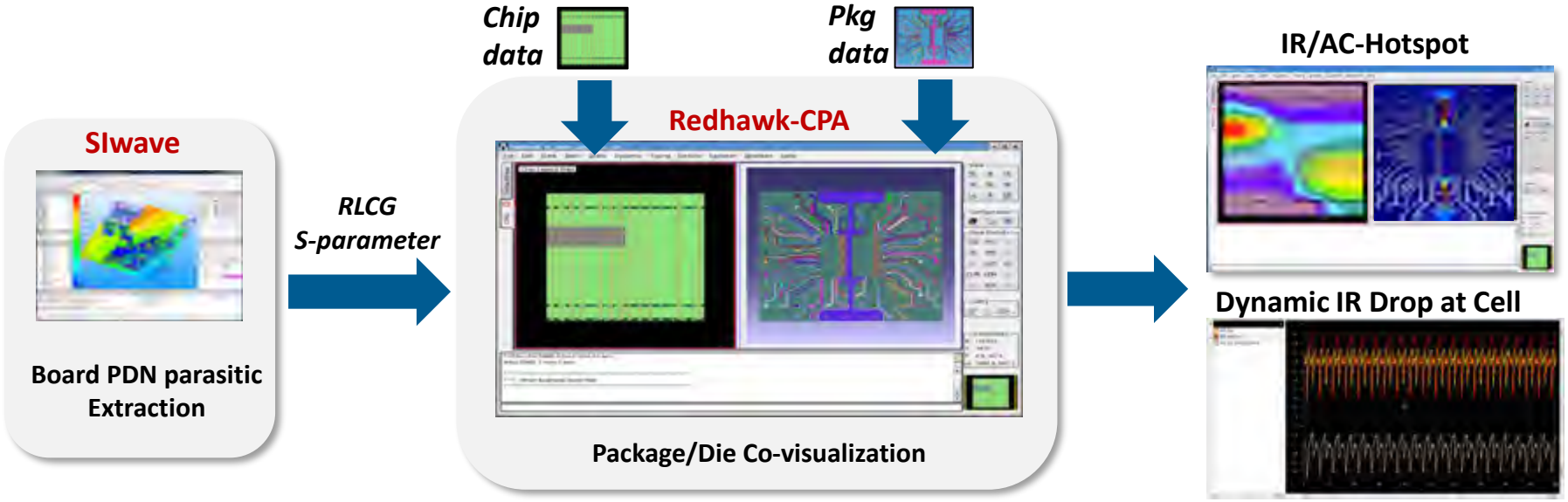
Manual Connection

ANSYS Chip Package System Convergence

Power, Thermal, Reliability, EMI and SI

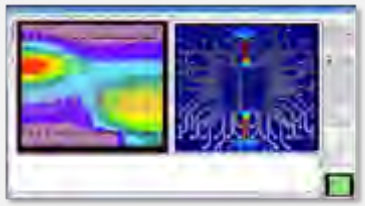


System Aware Chip Level Power Integrity Analysis



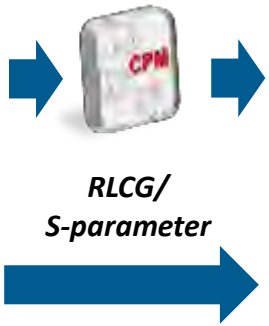
- Involved ANSYS products: SIwave, Redhawk/Totem-CPA
- Chip-Aware Package AC/DC hotspot => Optimization
- Board & Package aware IR/DvD

Chip Aware System Level Power Integrity Analysis

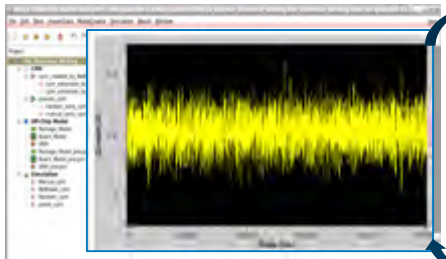


Redhawk-CPA

Package/Board in SIwave

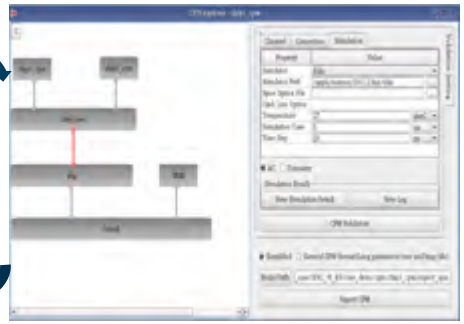


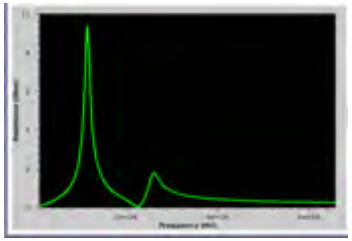
ANSYS CMA
(Chip Model Analyzer)



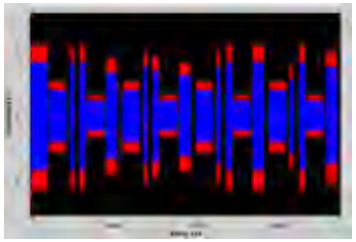
Full PDN CPM Creation

Full PDN Connection & Simulation





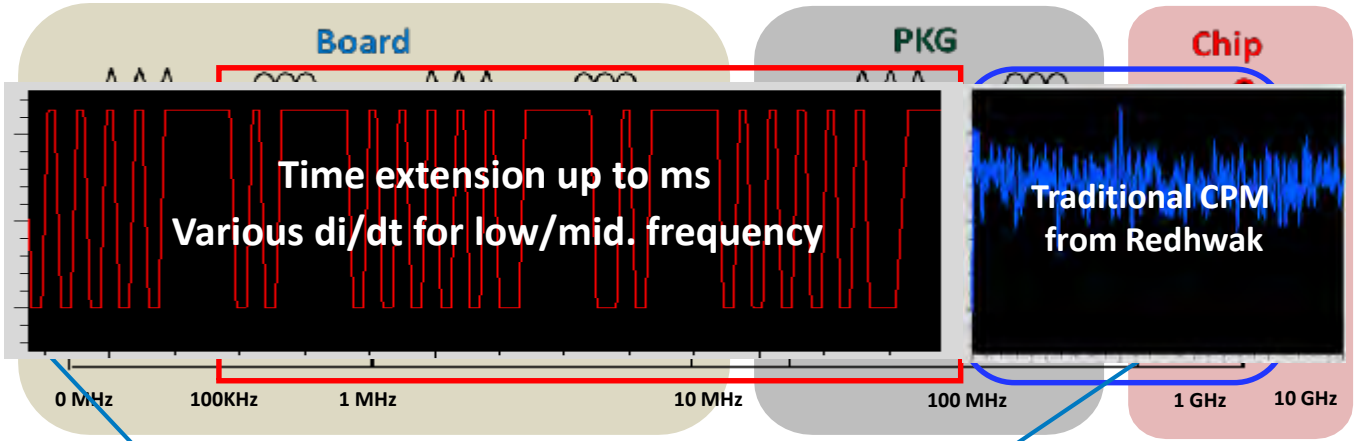
AC Analysis

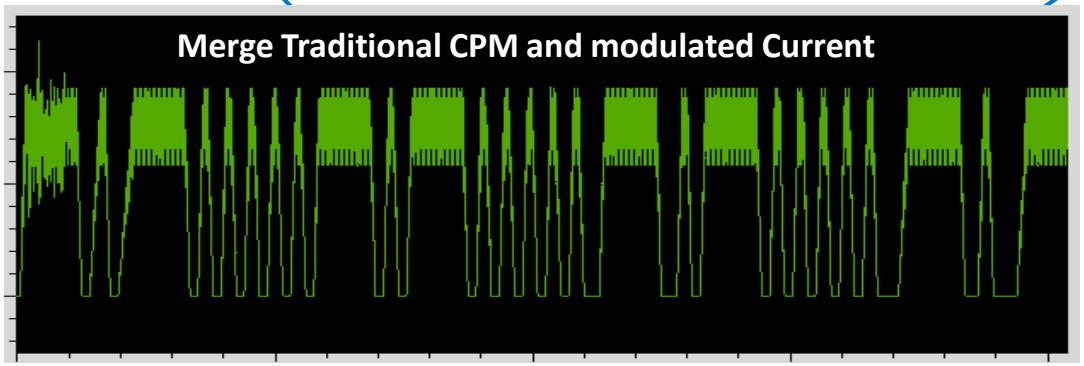


Transient Analysis

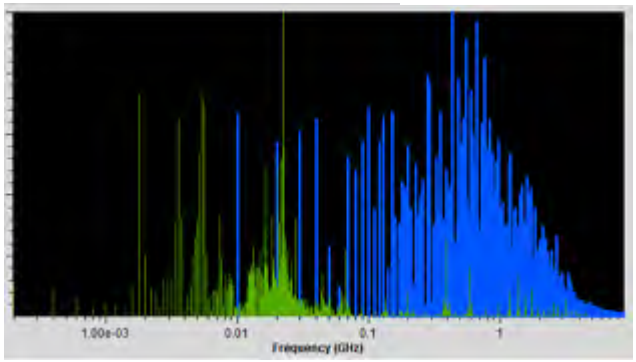
- Involved ANSYS productions: SIwave, Redhawk/Totem-CPA, ANSYS CMA
- Generates full PDN coverage current model
- Full PDN performance check through AC & transient simulation

Accurate Current Model for Full PDN Analysis





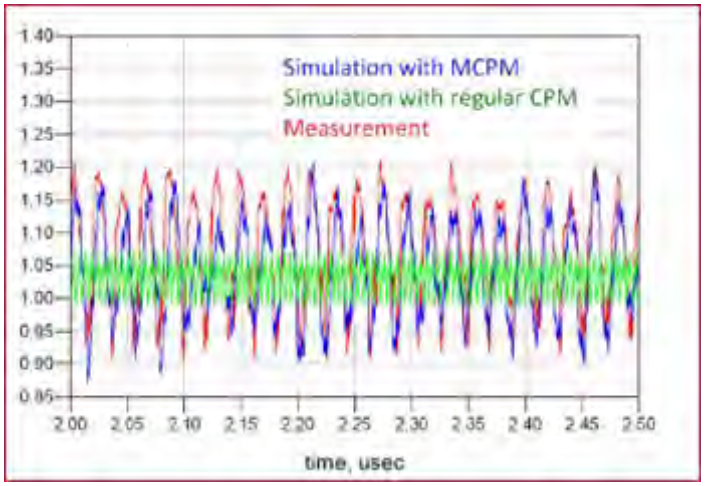
Full PDN Coverage Current Model from ANSYS CMA



Current Noise vs. CPM Types

System Level PI Analysis Case Study : CISCO & ST

Power Noise Detection & Mitigation with Full PDN Coverage CPM



Correlation Comparison vs. CPM types

Configurations	Description	Simulated noise [mV]	Measured noise [mV]
Test case 1	Baseline	384	356
Test case 2	Chip with additional 50% ODC	272	259
Test case 3	Chip with additional 50% ODC + Package cap count increased from 2 to 6	217	222

Voltage Drop Mitigation based on Full PDN Coverage CPM

- **Voltage drop(50mV) with regular CPM brings very optimistic result**
- **Only full PDN coverage CPM(=MCPM) detects severe power noise**
- **PDN can be only optimized by power noise analysis with full PDN CPM**

*** Sourced by Di Hu, Yongxue Yu, Antonio Ferrario, Olivier Bayet, "System Power Noise Analysis Using Modulated CPM", IEEE 2015**

Chip Aware System Level Signal Integrity Analysis

Package/Board in SIwave

RLCG/ S-parameter

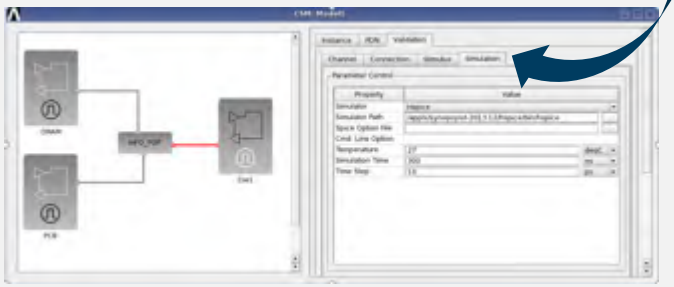
For IO Cell Characterization

IO Physical Design
(GDS/LEF/DEF)
IO Spice Netlist

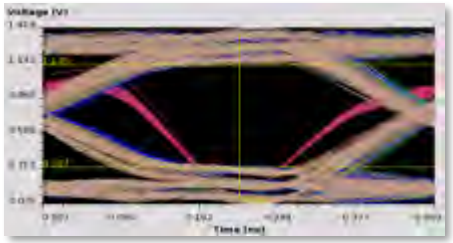
Ansys Chip Signal Modeling

IBIS/Xtor/CIOM
On-chip PDN
Intrinsic Cap of IO

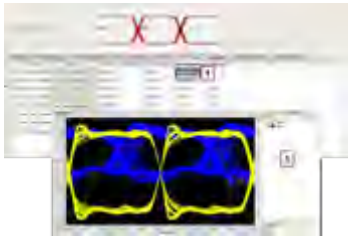
Chip Model Creation for Signal Integrity



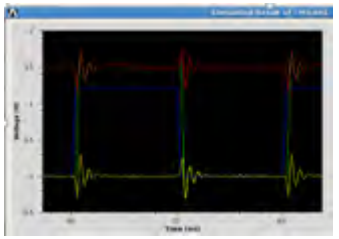
Channel Connection & Analysis



Jitter Analysis



JEDEC Timing Analysis



PG Noise Analysis

Accurate & Fast Chip Model for Signal Integrity

IBIS vs. Xtor vs. CSM

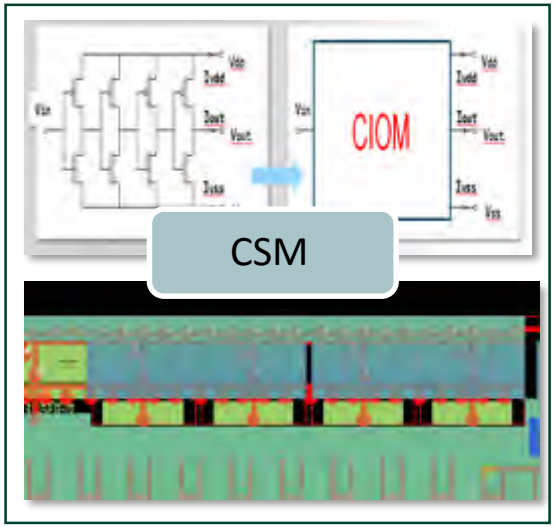
IBIS

- Easy to Handle
- Glitch
- Not Accurate
- Fast

vs.

Xtor

- Accurate
- Lack of capacity
- Long simulation
- Hard to get

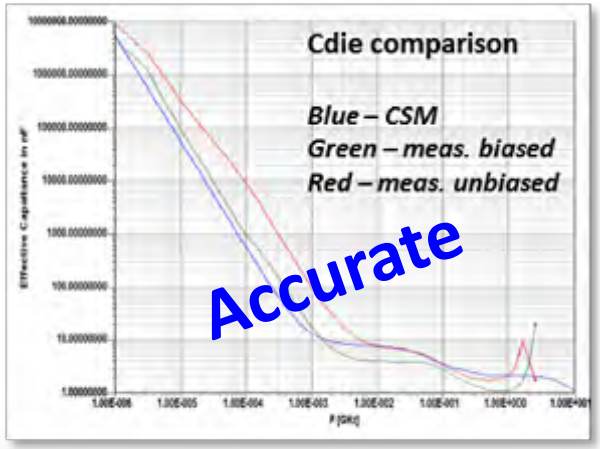


. Spice-level accuracy with full I/O bank capacity

. Captures impact of P/G noise on signal

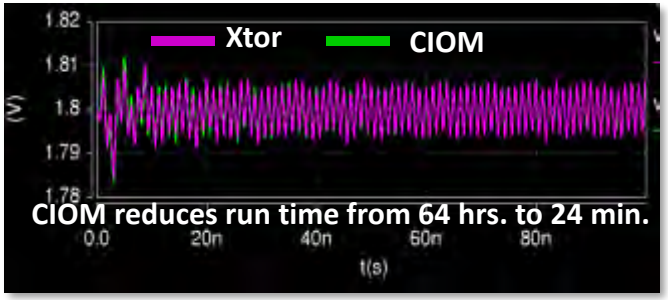
. IBIS/Xtor can be available in CSM

. Reduced grid can model thousands of nodes



Measurement correlated

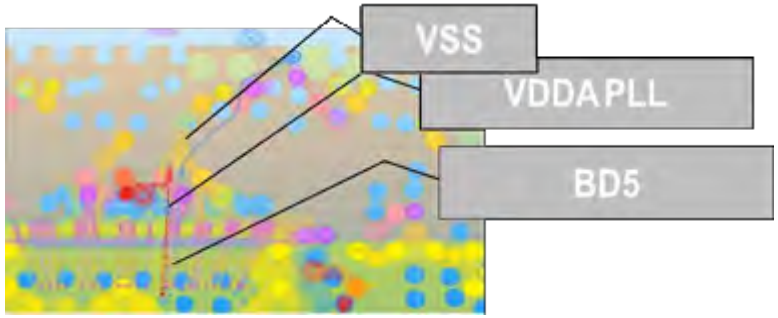
Fast & Accurate



Sourced by "System Level PDN Analysis Enhancement Including I/O Subsystem Noise Modeling" DAC 2013

System Level SI Analysis Case Study

Root Causing of PLL Failure and Guide Redesign of Chip-Package Routing

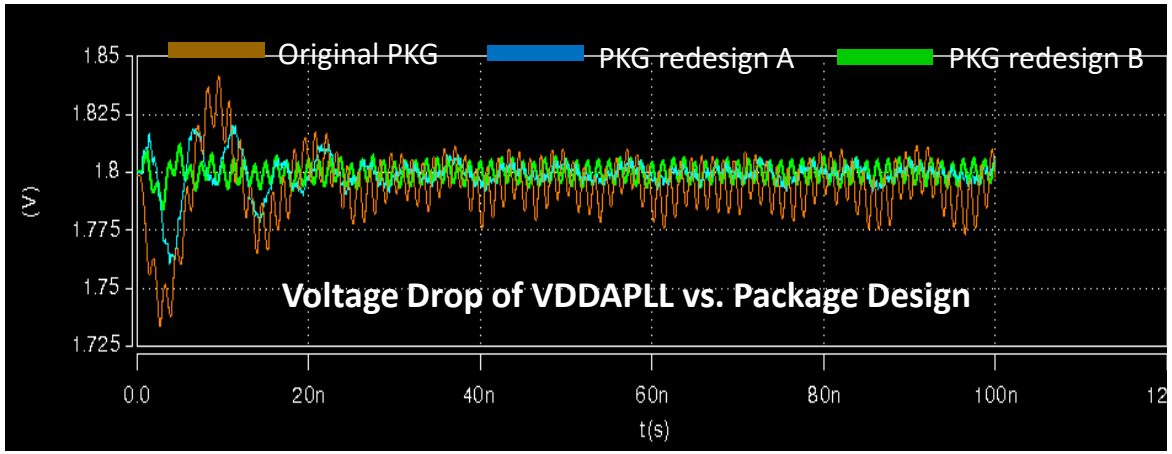


Original Package

Noise from DDR signal(B5) activity on PLL PG supply(VDDAPLL) results in PLL Failure(unlock)

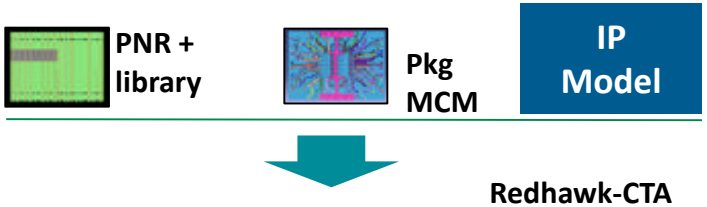
PKG redesign A: reducing impedance and ground bounce by merging PLL_VSSA to chip VSS

PKG redesign B: reducing impedance by shorting VDDAPLL with IO Power(VDDA1.8)

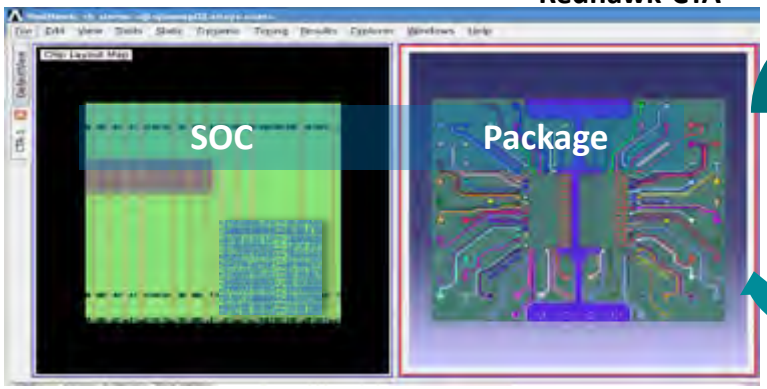


Sourced by "System Level PDN Analysis Enhancement Including I/O Subsystem Noise Modeling" DAC 2013

Chip-Package-System Thermal Aware Reliability Analysis

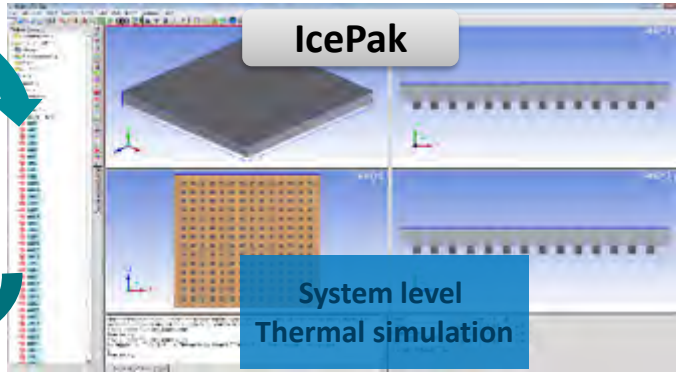


Redhawk-CTA

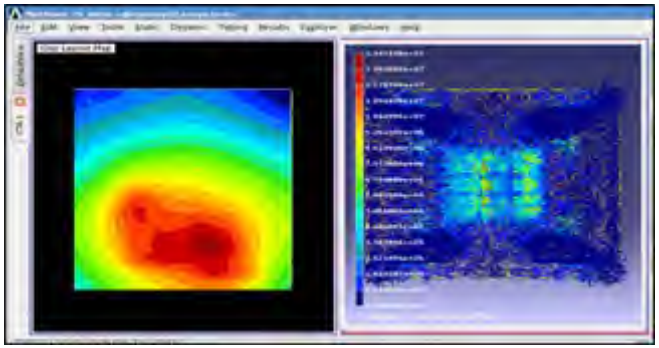


Chip Thermal Model(CTM)

Boundary conditions(HTC)



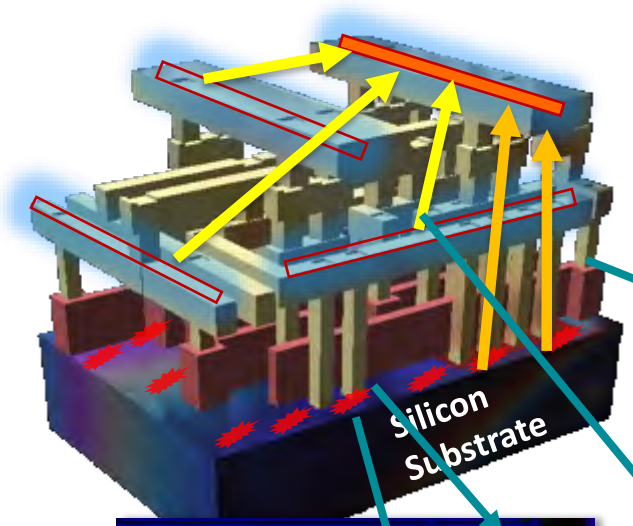
Generate Thermal Profile



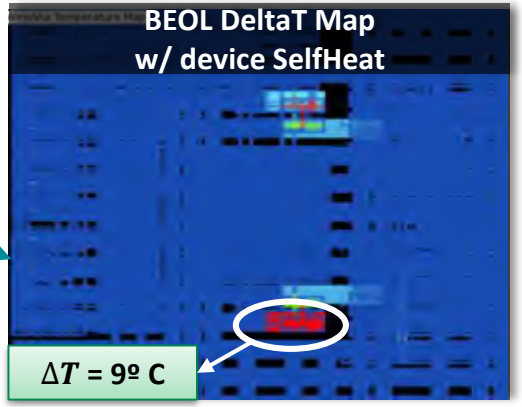
Back-annotation to chip
Thermal aware IR/DvD/EM/FIT Analysis

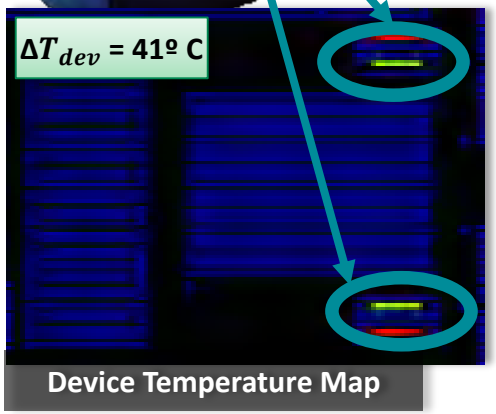
- Integrated Thermal/self Heat Analysis
- Full chip Capacity
- Seamless interface with IcePak
- Adv. Reliability(post-thermal EM , FIT)

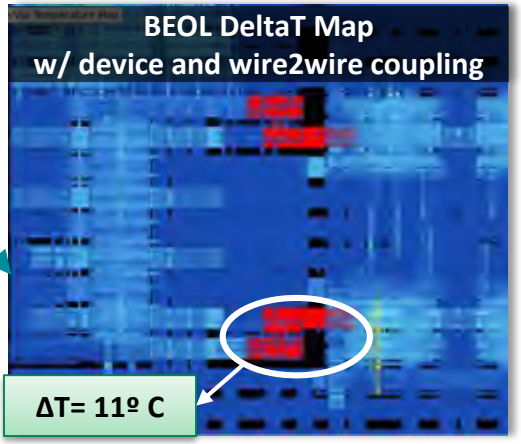
Case Study: Thermal-aware EM for Analog IP



$T_{ambient}$ = 100º C







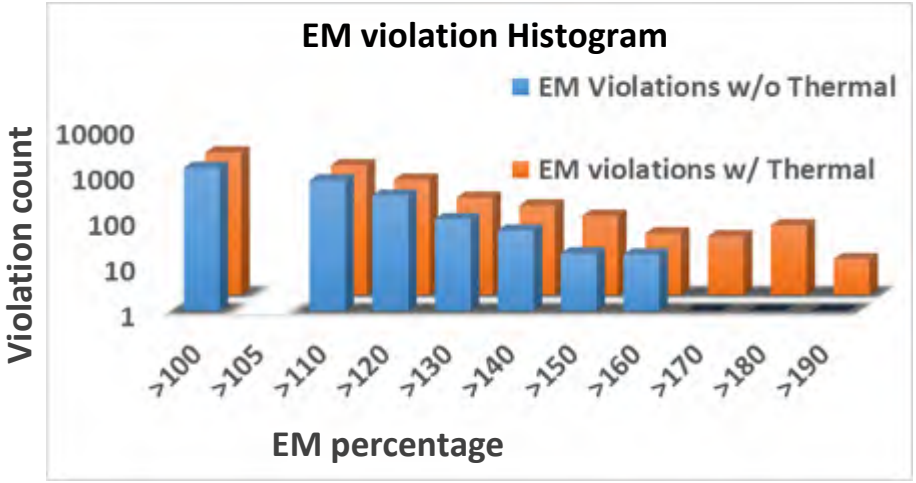
FIT Number
4.496e-1
4.788e2
1.283e3

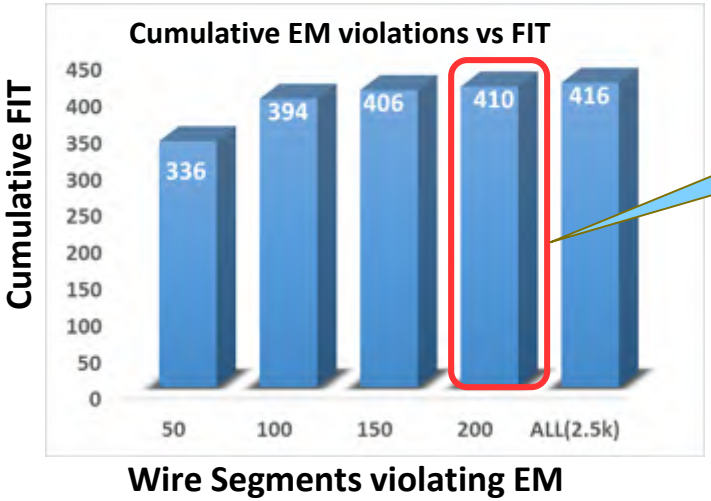
Thermal aware EM sign-off is a must for FinFET designs

Source: "A Thermal-aware Electromigration and Failure-in-Time Reliability Flow", Xilinx Inc., DAC 2017

Case Study: Thermal-aware Statistical EM for SoC

	T_{const}@ 105℃	T = 105℃ + ΔT
No. of EM violations	2581	2664
Max EM violation	168%	197%
Total FIT	23	416





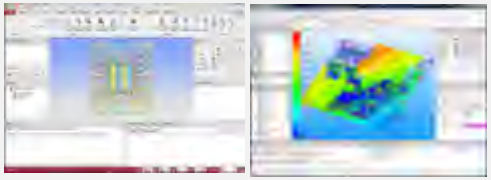
Top 200 violations → FIT of 410
So, Fix only 200 EM violations ☺

- SEB identify critical EM fixes
- Optimize for performance
- Improves productivity and TAT

"**Thermal-aware SEB for Advanced FinFET EM Sign-off**", Hisilicon Technologies, DAC 2017

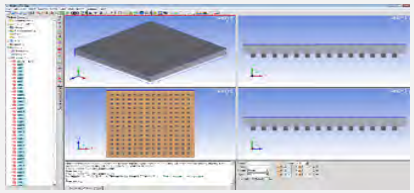
ANSYS Chip Package System Power/Signal/Thermal Integrity

SIwave



System Design Parasitic Extraction

IcePak



Chip & Package Aware HTC Generation

System Aware Chip Power Integrity	Chip Aware System Power Integrity	Chip Aware System Signal Integrity	Chip-Package-System Thermal & Reliability

Redhawk-CPA

Chip&PKG Co-analysis & visualization

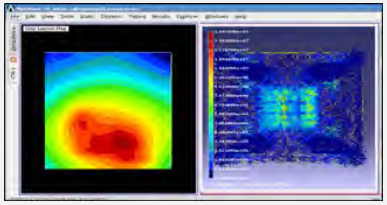
ANSY CMA

Full PDN CPM generation & Simulation

ANSYS CSM

Full Chip IO model generation & Simulation

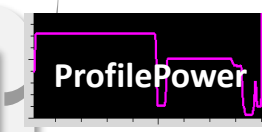
Redhawk-CTA



Package Thermal Analysis
EM & FIT Analysis

PowerArtist

RTL Power Estimation & Optimization



感谢聆听