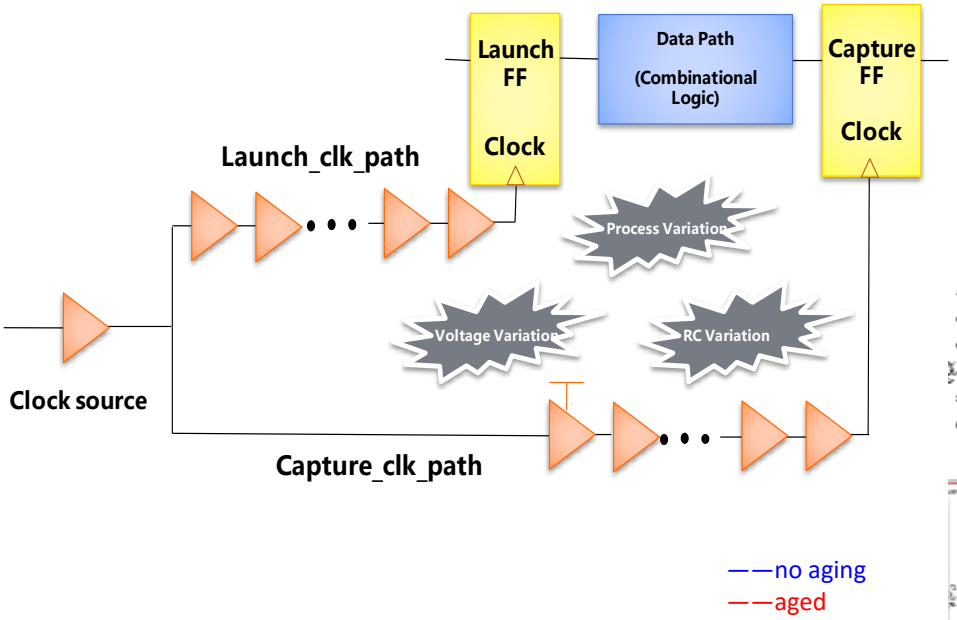
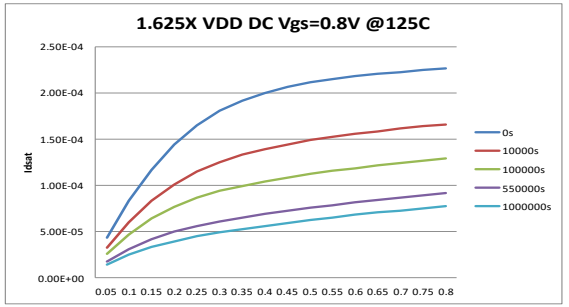
SOC Aging and EOS Solution

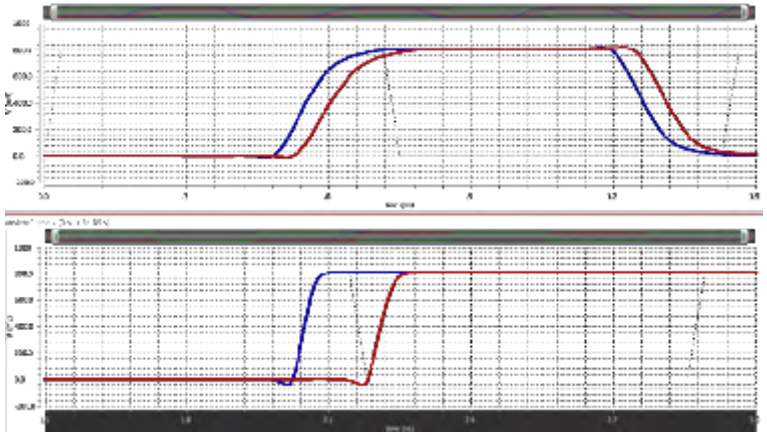
湛灿辉/Design For Reliability

Hisilicon

SOC aging

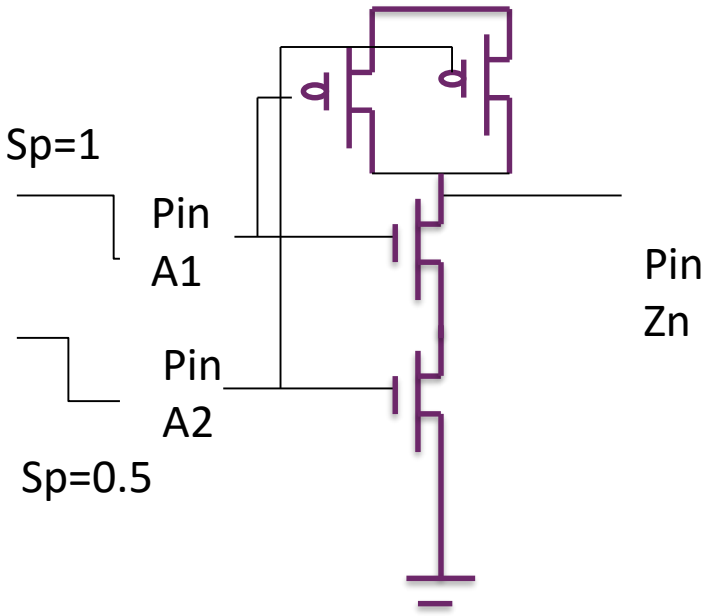




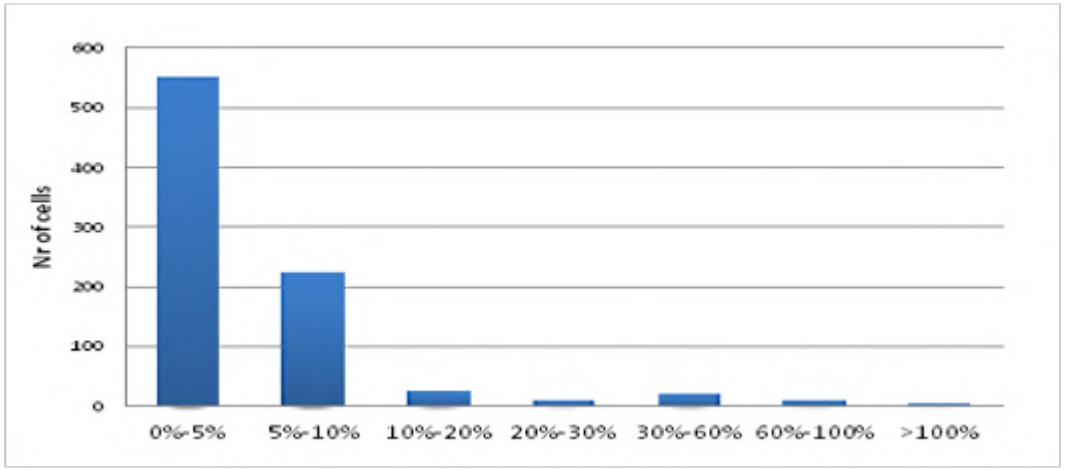


- Aging （HCI/BTI) will lead to timing violation after field application。

SOC aging



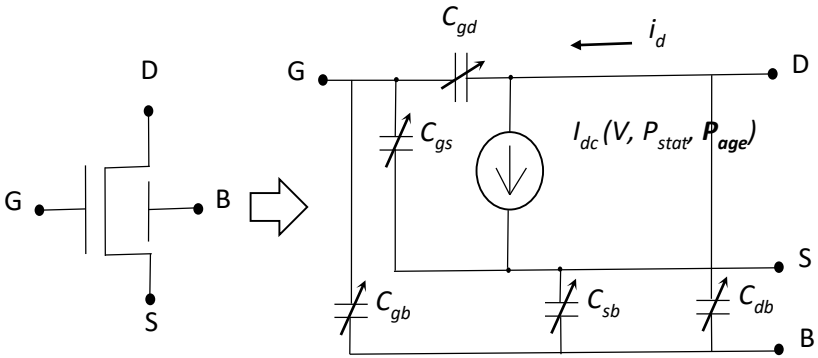
(a) **Input Sp impact on cell delay**



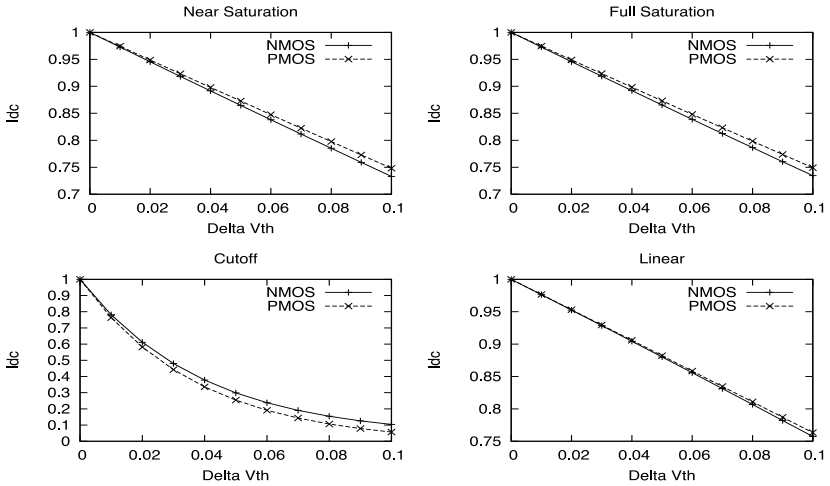
(b) Delay degradation % due to aging on cells in a library with SP=0.1 and 0.9

- **Aging library is not cover SP effect lead to 10% error.**

SOC aging

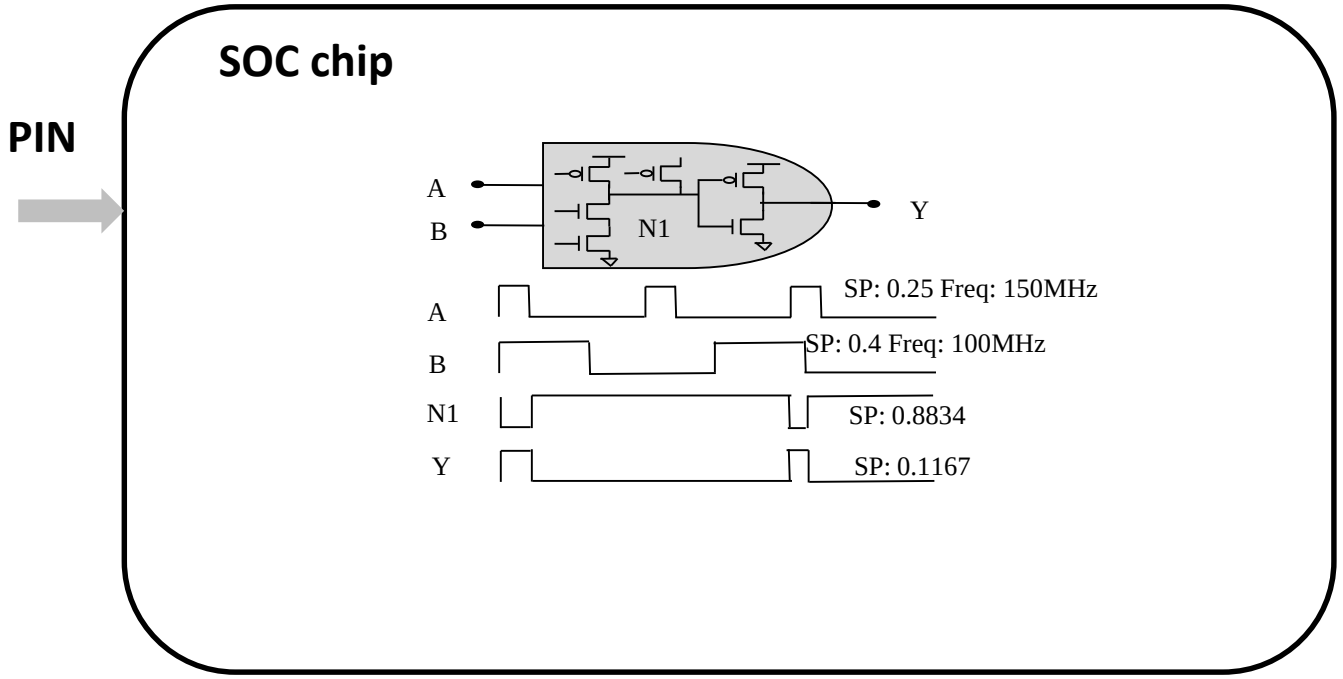


$$I_{dc\,sens}(V) = \left\{\frac{\partial I_{dc}(V)}{\partial P_{age\_deltavth}}\right\}$$



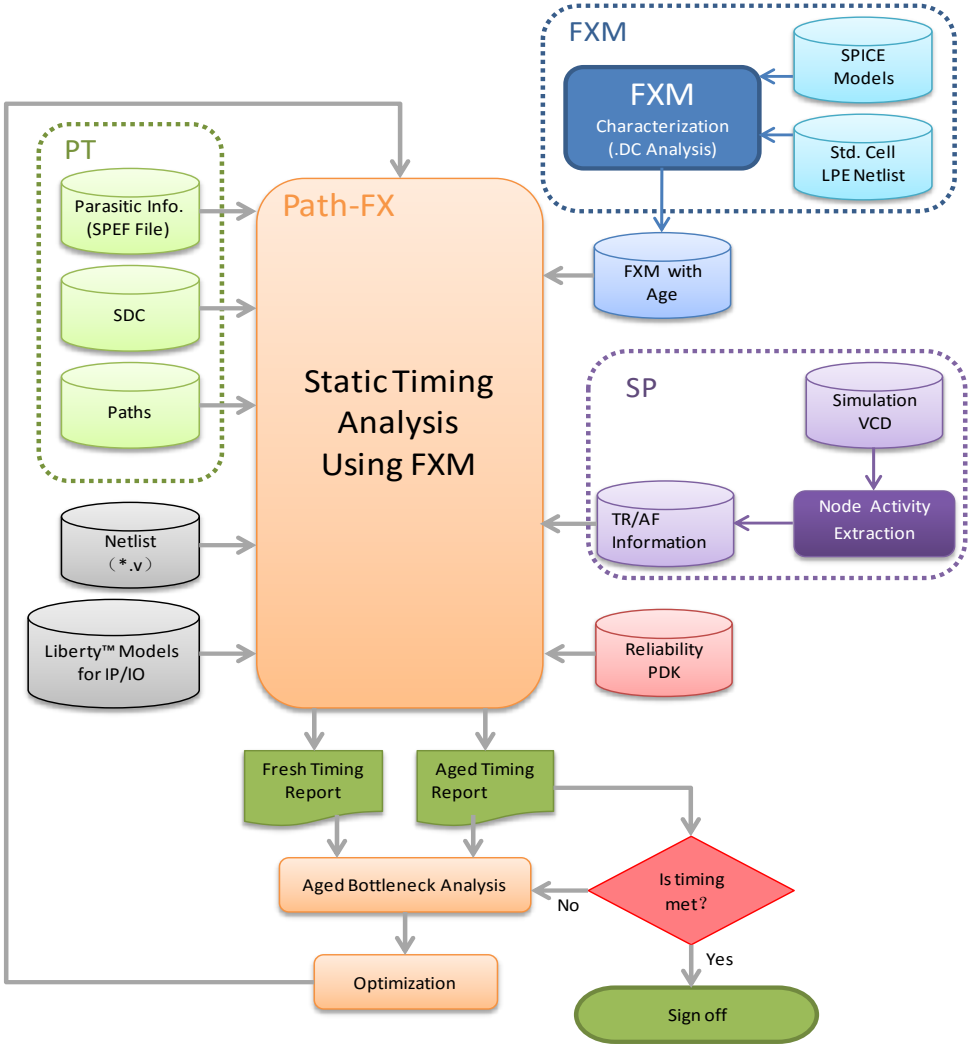
- **A new SOC Chip Level Aging Timing Sign-off Solution based on Ansys FXM and Path-FX™ is introduced.**
- **Path-FX™ is a path timing analysis tool that uses the FXM to perform fast SPICE-like simulation. It's a Transistor level STA, so the variation of transistor can be involved in STA easily.**

SOC aging



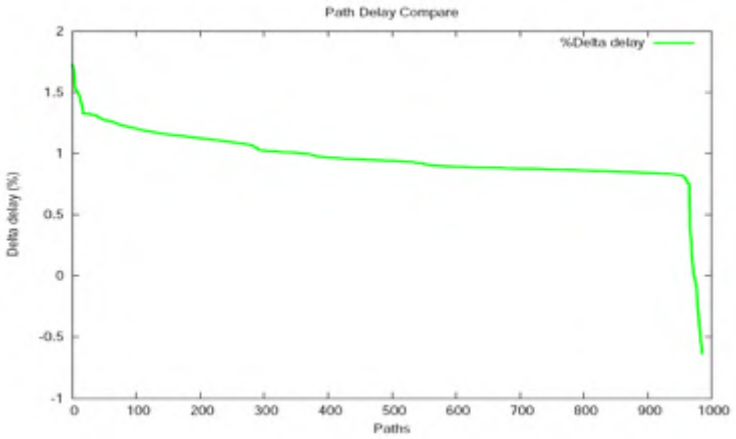
- Capture the pin SP of each cell by VCD or static method.
- Propagate the SP to each transistor in the cell.
- Calculate age_deltavth=F{ MTTF,Vgs,T,L ,sp,frequency, device type}

SOC aging

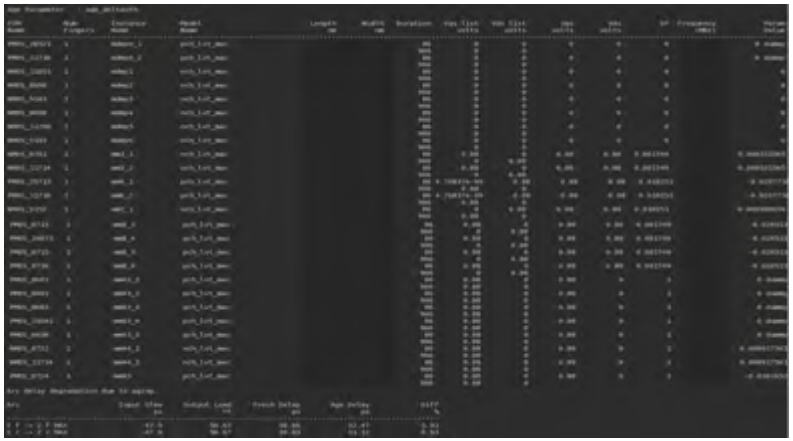


- **The solution has:**
- **1. Spice-like paths aging simulation**
- **2. Unique aging degradation for each device/cell which dependents on its workload in path;**
- **3. Fast runtime**

SOC aging



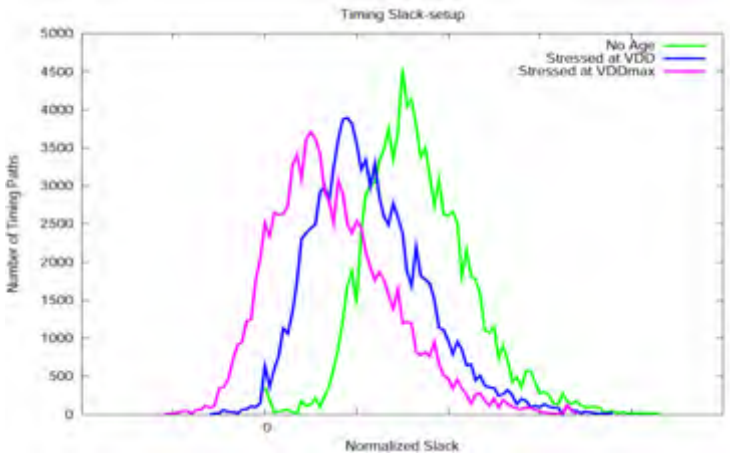
Timing path delay comparison between Path-FX versus Spectre™

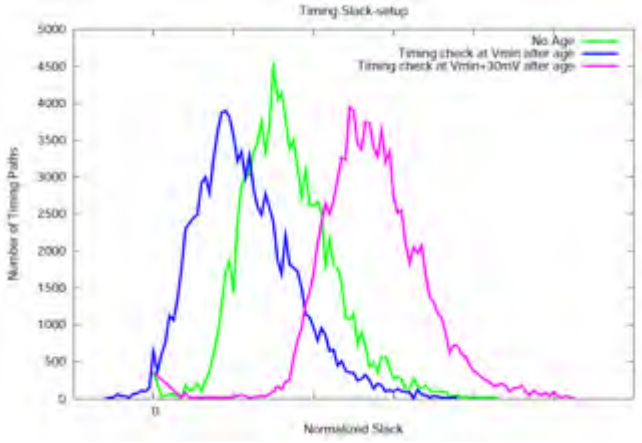


SP dependent transistor aging degradation in path

- **A commercial sub-16nm, ~ 0.3Billion gate count network chip is used for aging timing sign off with the methodology. 1,000 paths are selected randomly to do SPICE Spectre™ simulation to show the accuracy of the methodology(<2%). It takes 6 hours for 100,000 paths' setup aging timing check in one corner with 30 processors.**

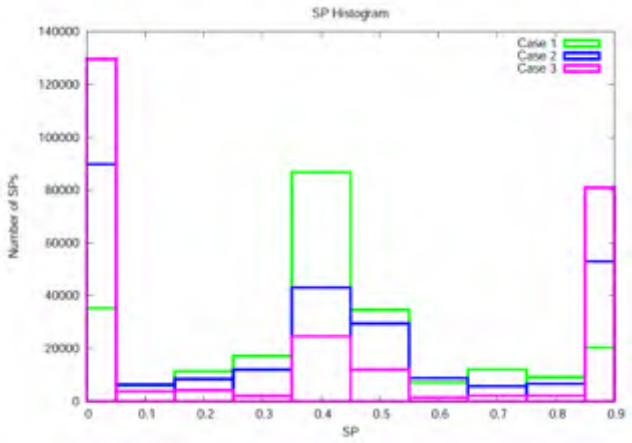
SOC aging

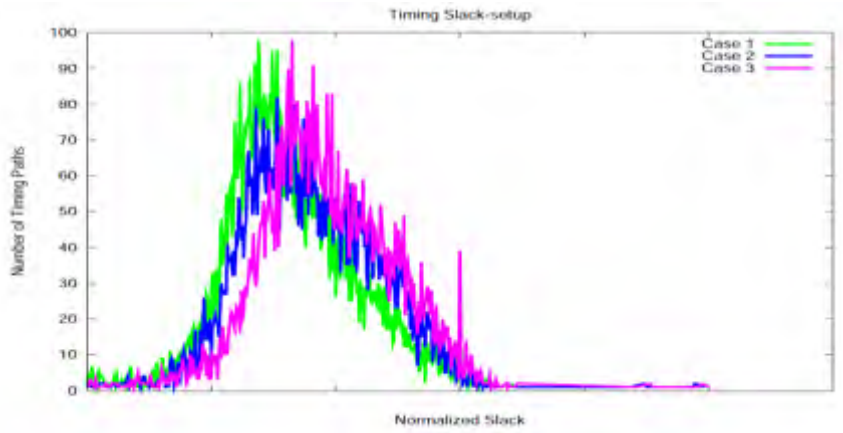




- **If increasing the stress voltage at VDDmax, the distribution of the setup timing slack will shift on left more, hundreds of paths instead of tens of paths appear timing violation;**
- **It is easy to get the Vmin or Fmax after lifetime；**

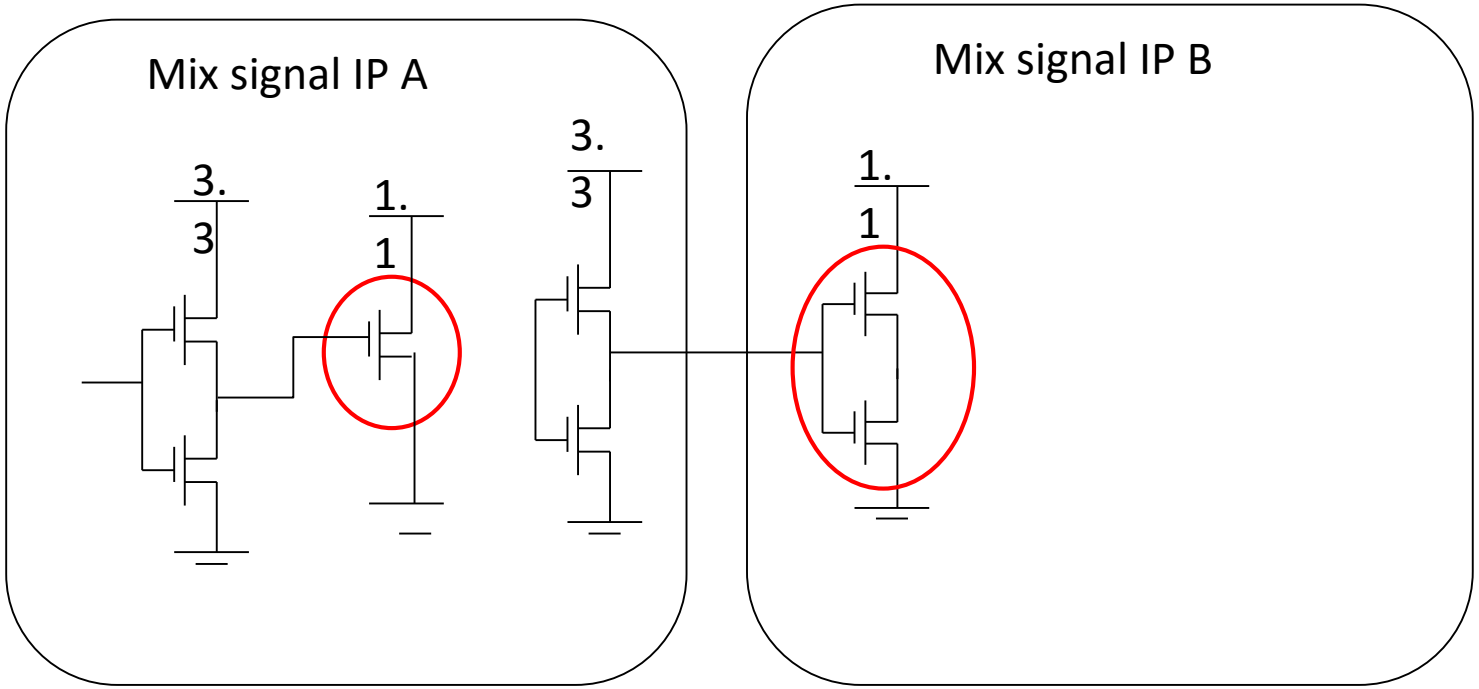
SOC aging





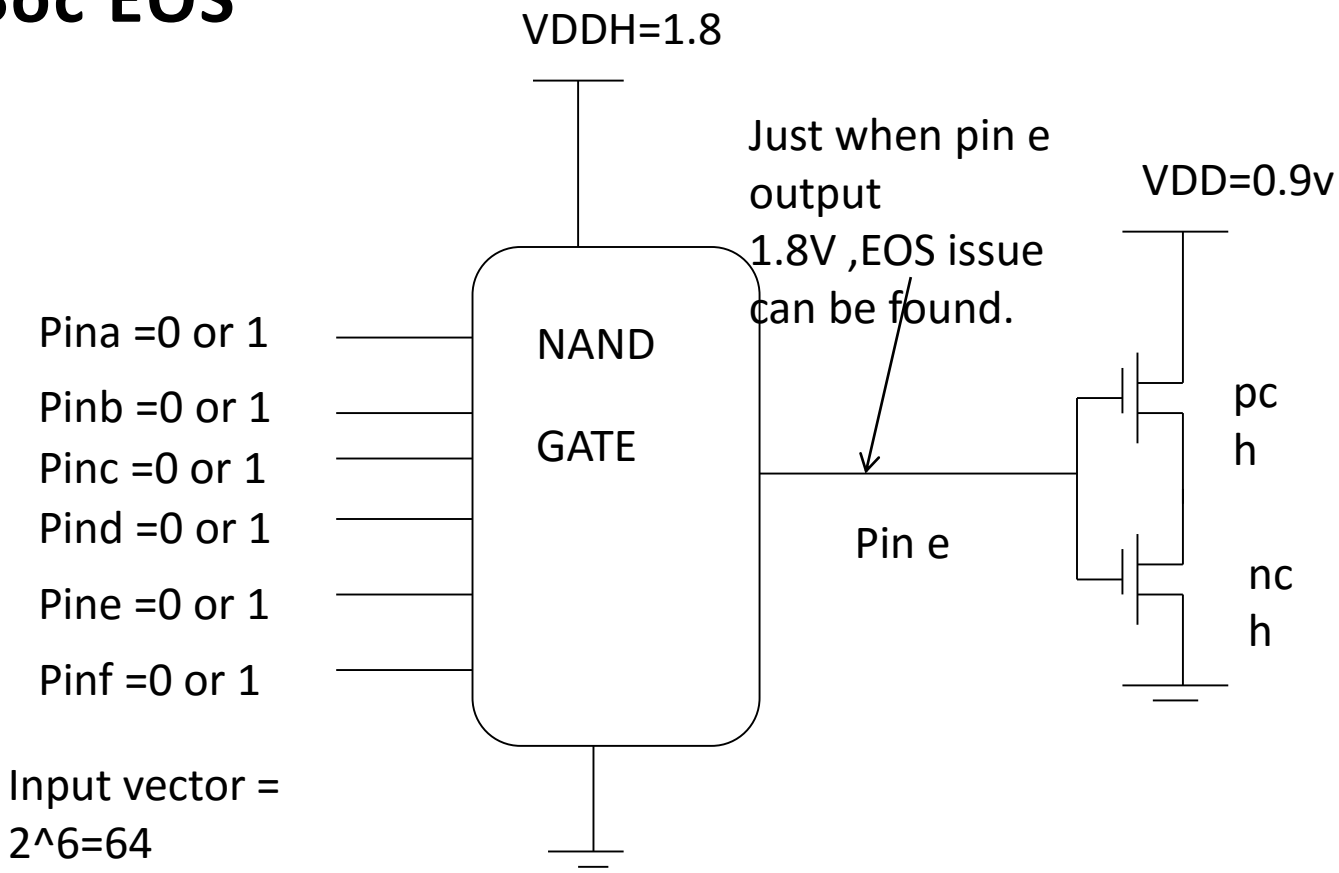
- **Three different simulation scenarios of a module are selected to show the impacts of SP on aging timing**

Soc EOS



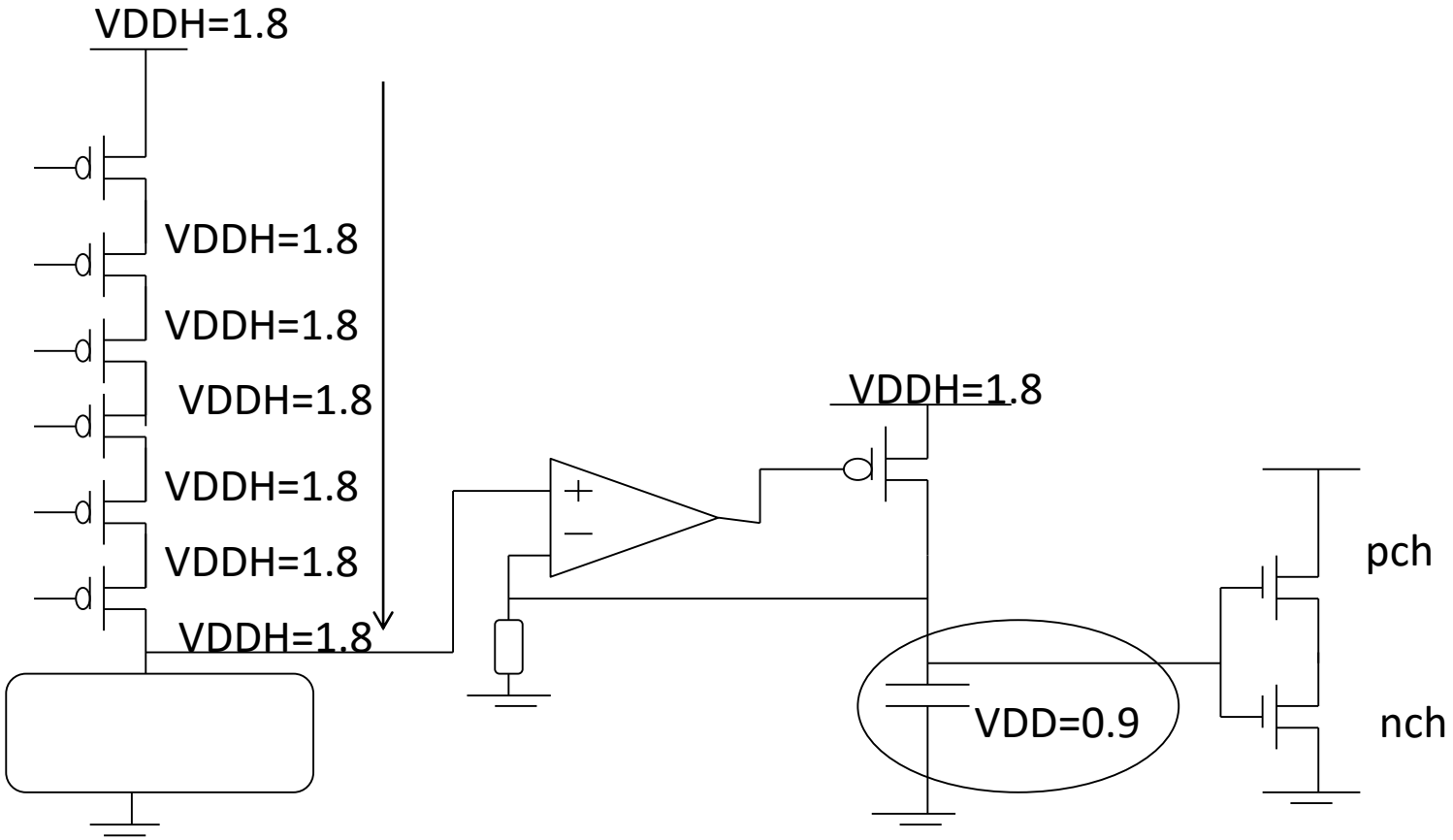
- **Muti power domain design is easy to induce EOS (electrical overstress) failure**
- **Chip will be fail in field application.**

Soc EOS



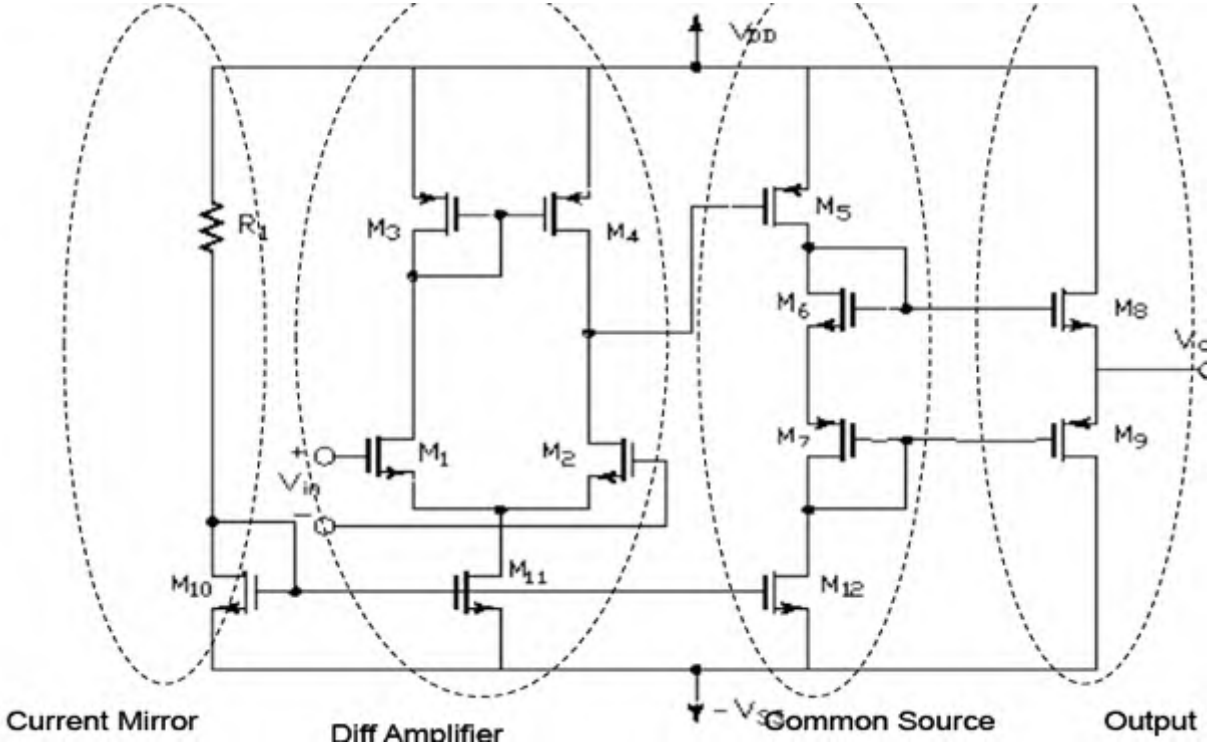
Simulation check will miss violation for input vector coverage

Soc EOS



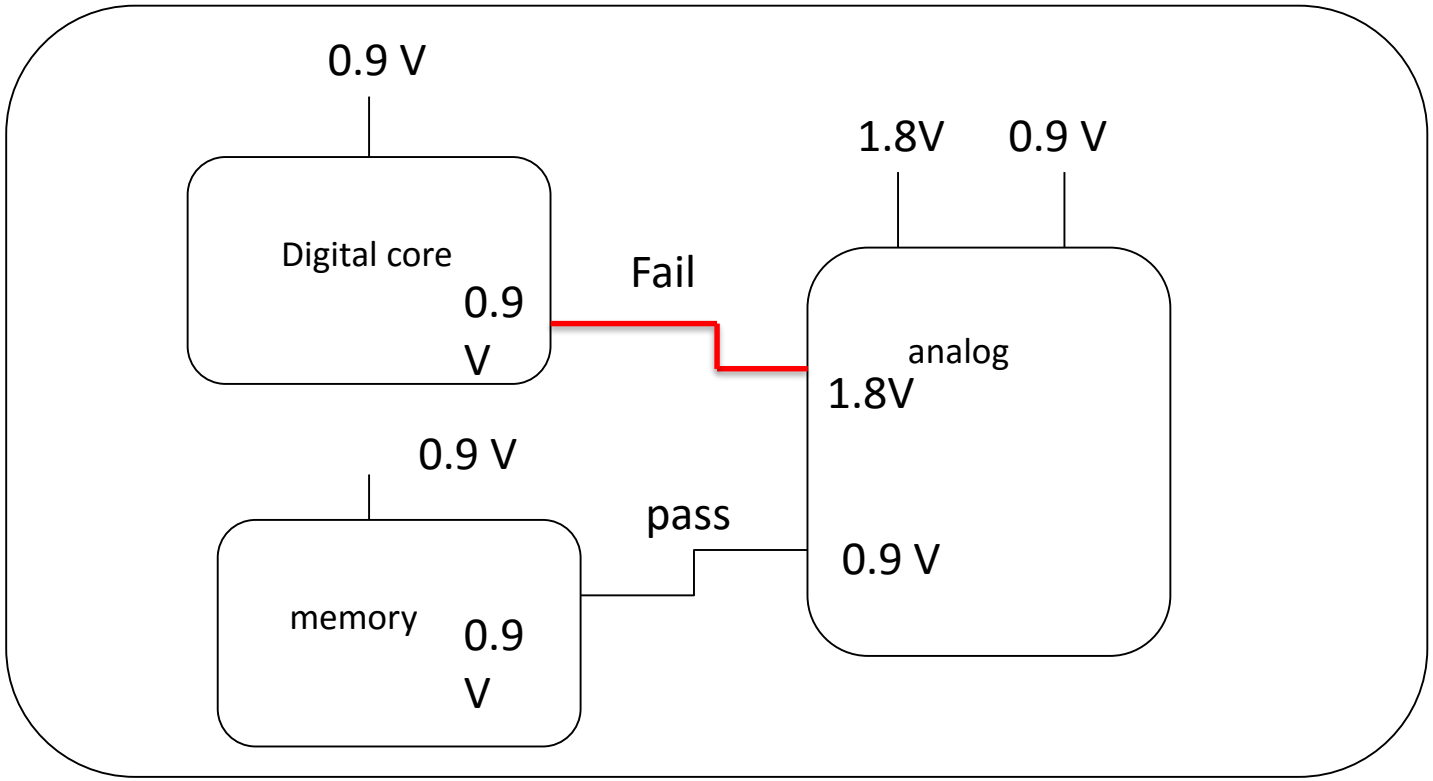
- **Voltage propagate can cover all the violation but with much fault violation**

Soc EOS



- **EOS_FX solution can cover all the violation but little fault violation**
- **It run partition on the circuit and simulate all the input vector of each part.**

Soc EOS



- **Run EOS_FX in IP block and check each device.**
- **Check interconnect of each block interface in SOC level.**

感谢聆听