Ensuring ESD Robustness for IPs and SoCs

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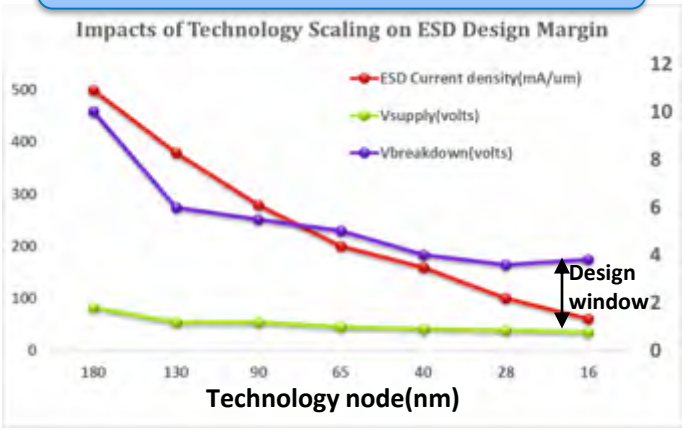
Analogix

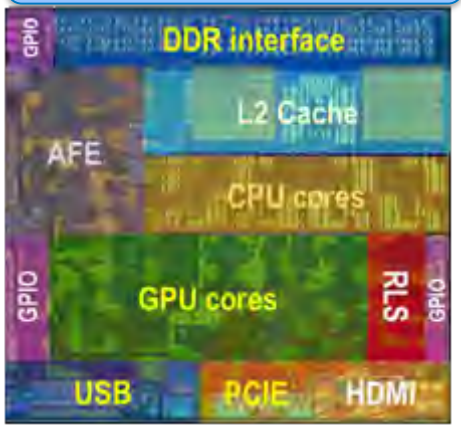
Challenges in ESD Design

Shrinking Design Margins



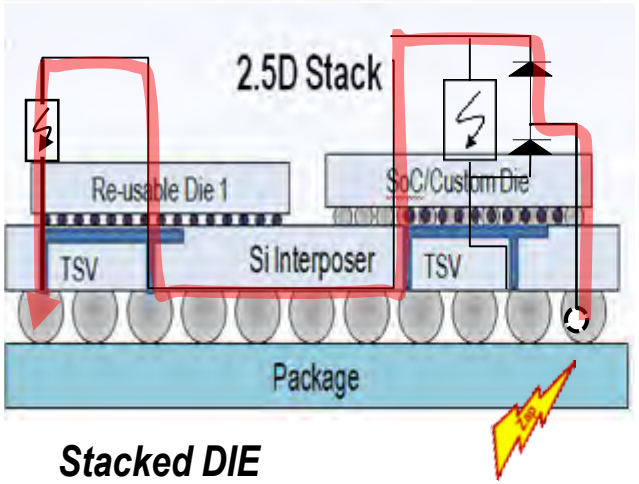
Thinner oxides
Thinner Interconnects
Smaller devices

Higher Integration



Power/Ground islands
Unique ESD requirements
Higher pin-counts

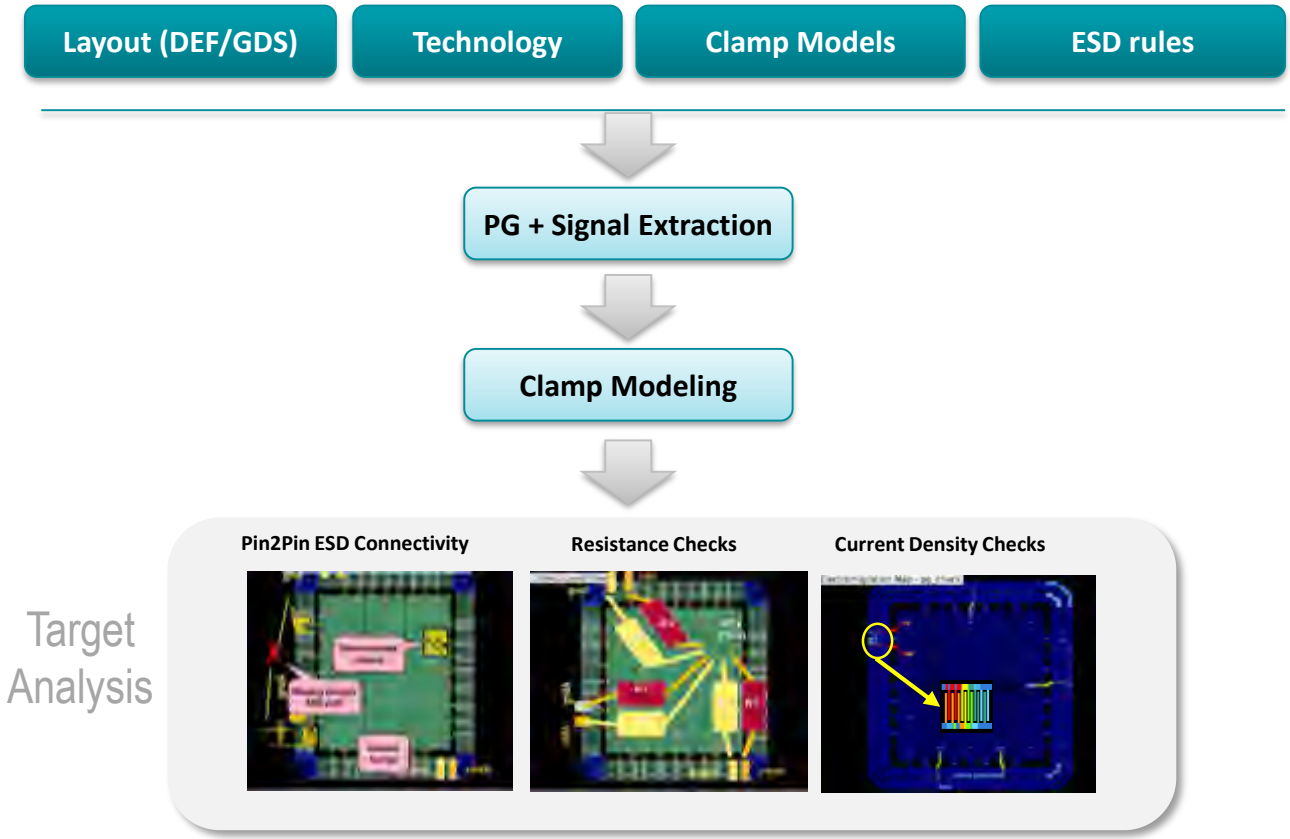
Evolving Technologies



Stacked DIE
HBM, Memory Cube
System in Package

Systematic ESD verification is a must to ensure first silicon success

ANSYS PathFinder™: SoC and IP ESD Integrity



Analogix use pathfinder for ESD sign-off

ESD connectivity check

- *Do we have unconnected Clamp Instance ?*
- *Do we have bumps isolated from Clamps ?*
- *Do we have proper stage of ESD connectivity for each net-pair ?*

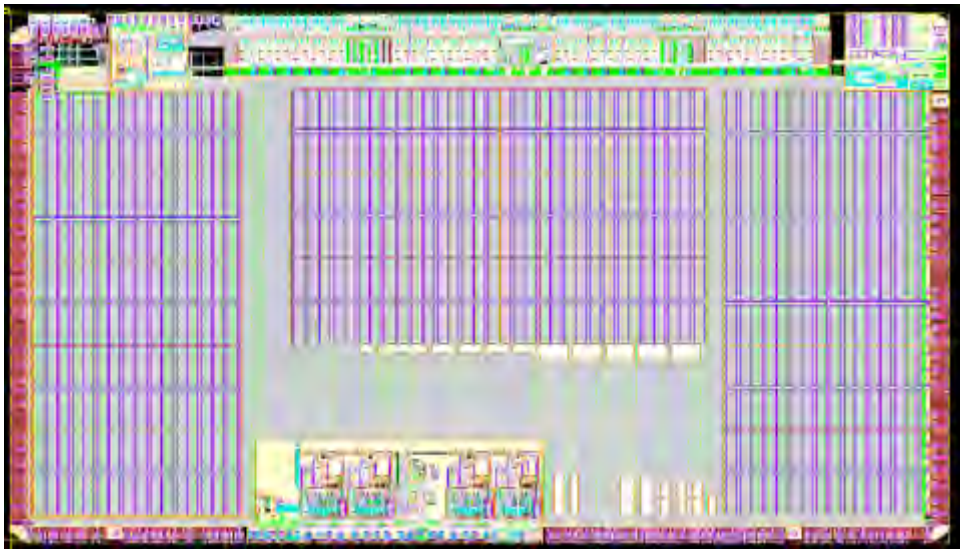
Rule based Resistance check

- *Is our ESD path's resistance small enough to protect function circuit ?*

Rule based Current Density check

- *Is our ESD path's routing strong enough to bear big ESD discharge current ?*

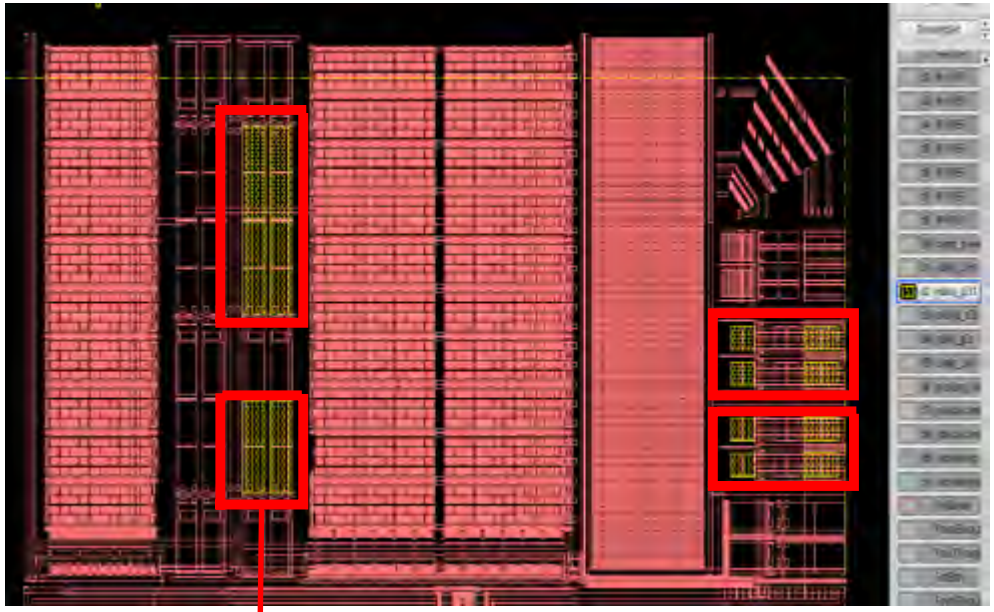
Analog case overview



Process	TSMC 28HPC+
Size	6350umx4770um
No. of Bumps	• ***259 Bumps*** ***-14 Power*** ***- 16 Ground*** ***- 65 Signal***

How to recognize ESD cell ?

- Drawing corresponding GDS mark layer on ESD cell （ clamp/diode ）



```
M5        m 35:0    135:0
VIA5      v 55:0    -
M6        m 36:0    136:0
VIA6      v 56:80   -
M7        m 37:80   137:0
VIA7      v 57:80   -
M8        m 38:80             138:0
RV        v 85:0;76:0    -
AP        m 74:0    126:0
prboundary b 108:0 -
CPWR    ESD    256:1 -
PDS2P    ESD    256:2 -
NDG2S    ESD    256:3 -
PNDB2B    ESD    256:4 -
PDG2P    ESD    256:5 -
PCMP_SOF    ESD    256:7 -
LOCALPCMP_SOF    ESD    256:8 -
```

Mark layer can be used for Both the ESD and device identification purposes in GDS2DB

Define different layer number in GDS layermap to identify different ESD cells

How to model ESD cell ?

1. Use R-ON/R-OFF model to define each type of ESD cell

```
BEGIN_CLAMP_TYPE
CLAMP_TYPE PCMP_SOF
CELL_NAME anx_maple_chip_PCMP_SOF_*
PIN_TYPE pwr AVDD10_ck AVDD10_data AVDD18_PAD AVD
1V01_PAD DVDD1V23_PAD DVDD_PLL PAD_PVIN PAD_SVIN
PIN_TYPE gnd AVSS10_ck AVSS10_data AVSS18_PLL AVS
AVSSIO_PAD AVSS_VCO DVSS1V01_PAD DVSS1V23_PAD DVS
BEGIN_PIN_TYPE
NAME pwr
SHORT 1
END_PIN_TYPE
BEGIN_PIN_TYPE
NAME gnd
SHORT 1
END_PIN_TYPE
PIN_PAIR pwr gnd 0.1 off
END_CLAMP_TYPE
```

```
BEGIN_CLAMP_CELL
    NAME  <cell name>
    TYPE <user_type_name>
    ? PIN [<pin_name> | NA] [<x_loc> <y_loc>]
        [ BOTTOM | TOP |<layername>] <locID> ?
    ? XTOR <xtorName>:<net> <x_loc> <y_loc> <layer> <locID> ?
        ...
    ? RON <clamp_On_Resistance_Ohms> ?
    ? ESD_PIN_PAIR <loc_ID1> <loc_ID2> [
        [ <Ron> | [ <Ron+>|OFF] [<Ron->|OFF] ]?
        <I-V_clamp_name> ]?
    ? IMAX <I1> [<I2>] ?
    ? VMAX <V1> [<V2>] ?
    ? RAIL_VOLTAGE <voltage> ?
END_CLAMP_CELL
```

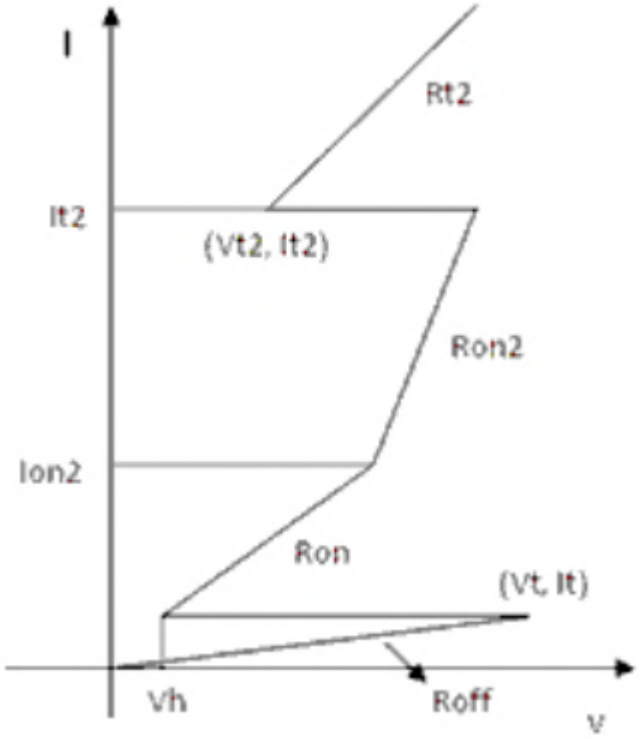
Resistance value is 0.1Ω when clamp is on,When current from gnd to pwr, clamp is off

Defines legal ESD discharge path and resistance values for both current discharge directions

How to model ESD cell ?

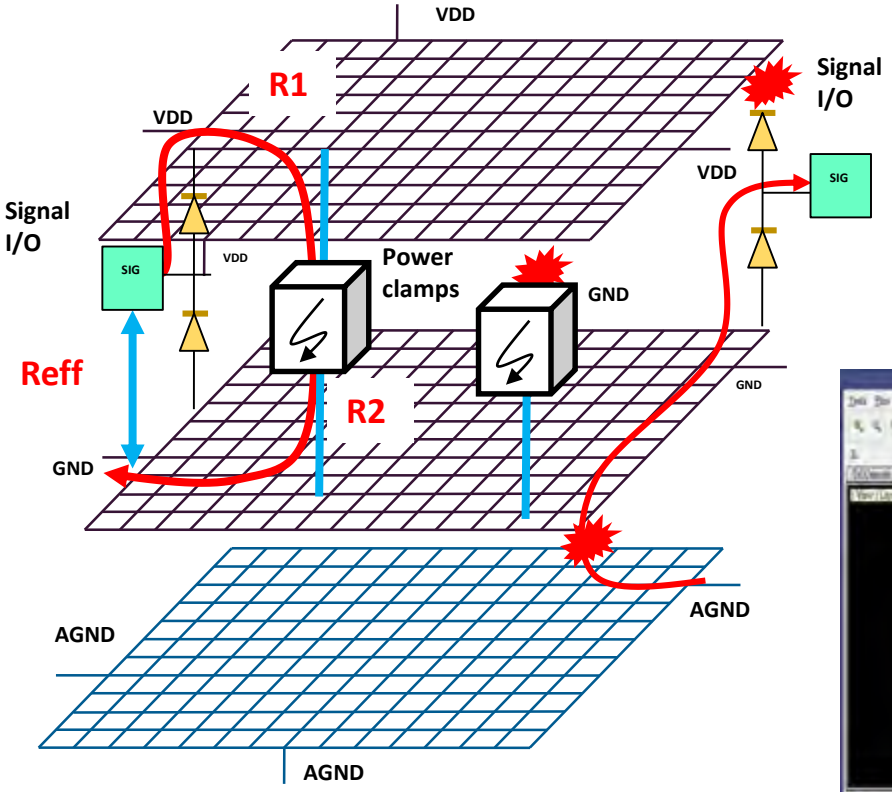
2. Use IV-Curve to define each type of ESD cell

```
BEGIN_CLAMP_IV
  NAME <name of I-V clamp>
  Ron <Ron+> [<Ron->]
  VT1 <VT1+> [<VT1->]
  VH <VH+> [<VH->]
  ROFF <Roff+> [<Roff->]
  ION2    0.9
  RON2    0.1
  IT2     3.0
  RT2     1.0
  VT2     0.5
END_CLAMP_IV
```



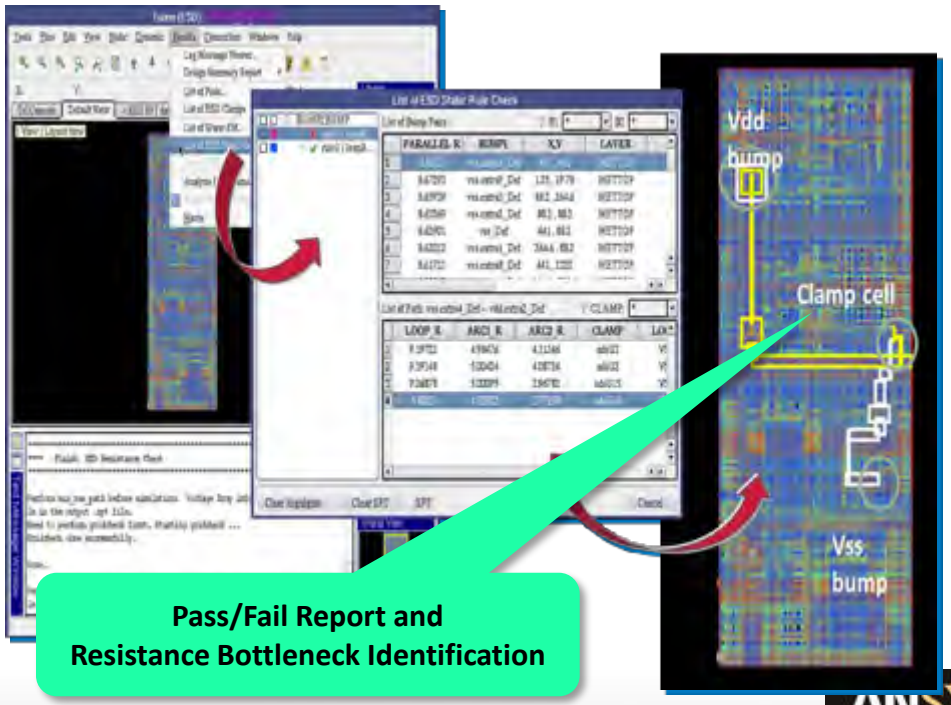
All clamp cells are modeled as resistors with IV curve

ESD Connectivity and Rule Checks



- Full SoC Capacity
- Multi-threaded solve
- Simple and customizable rules

- Isolated Bumps/Clamps Checks
- Pin2 Pin ESD Connectivity Checks
- Pin2Pin Resistance Checks
- Layout-based Debug



ESD Connectivity Check

- **List of Bumps Isolated from Clamps**

```
######### List of Bumps Isolated from Clamps ##########
#
# <BUMP_NAME> <BUMP_X> <BUMP_Y> <BUMP_LAYER> <NET_NAME>

AVDD18_PAD_Def  2786.24 -10.07  AP      AVDD18_PAD
AVDD18_PAD.extra1_Def   1881.84 3.515   AP      AVDD18_PAD
PAD_PVIN_Def    5993.11 4431.71 AP      PAD_PVIN
PAD_PVIN.extra1_Def     5993.11 4246.45 AP      PAD_PVIN
PAD_PVIN.extra2_Def     5993.11 4340.5  AP      PAD_PVIN
PAD_PVIN.extra3_Def     6060.52 4340.5  AP      PAD_PVIN
PAD_PVIN.extra4_Def     6060.52 4246.45 AP      PAD_PVIN
PAD_PVIN.extra5_Def     6060.52 4431.71 AP      PAD_PVIN
```

Bumps doesn't have connections to clamp cell will be reported as shown, includes bump name/location/layer /net name

ESD Connectivity Check

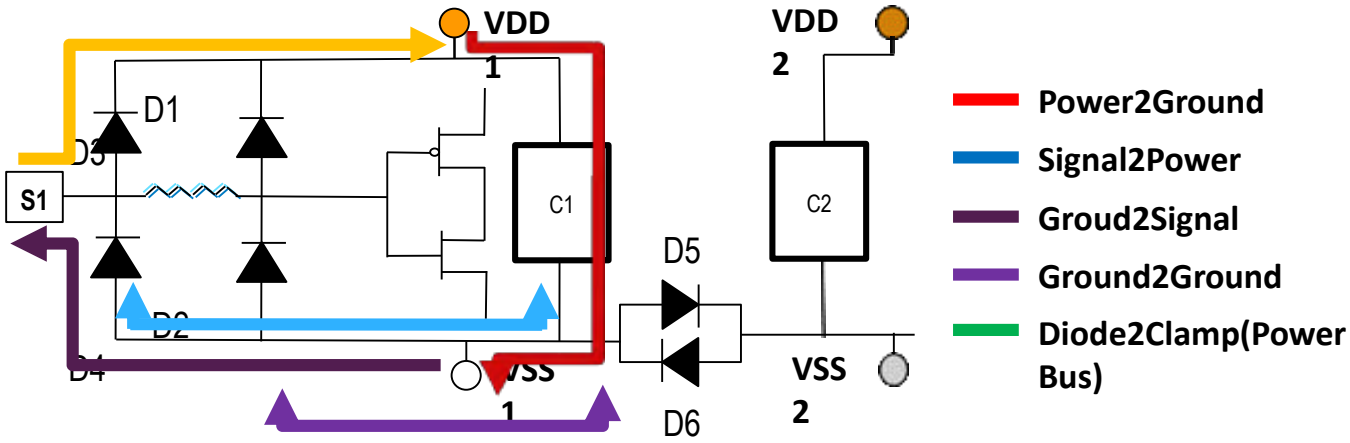
- **Net-Pair ESD connectivity**

```
# Inquery all net pairs
Set maximum ESD stage to: 10
# Check connections of <10> stage
#
# <NET1> <NET2> <MIN_ESD_STAGE> <MAX_ESD_STAGE>

AVDD10_ck -> AVDD10_data - -
AVDD10_data -> AVDD10_ck - -
AVDD10_ck -> AVDD18_PAD - -
AVDD18_PAD -> AVDD10_ck - -
AVDD10_ck -> AVDD18_PLL - -
AVDD18_PLL -> AVDD10_ck - -
AVDD10_ck -> AVDD18_TX 2 4
AVDD18_TX -> AVDD10_ck - -
```

Reports the min/max ESD stage between ESD net pair
Minimum 2 stages and up to 4 stages ESD connection between AVDD10_CK and AVDD18_TX as shown

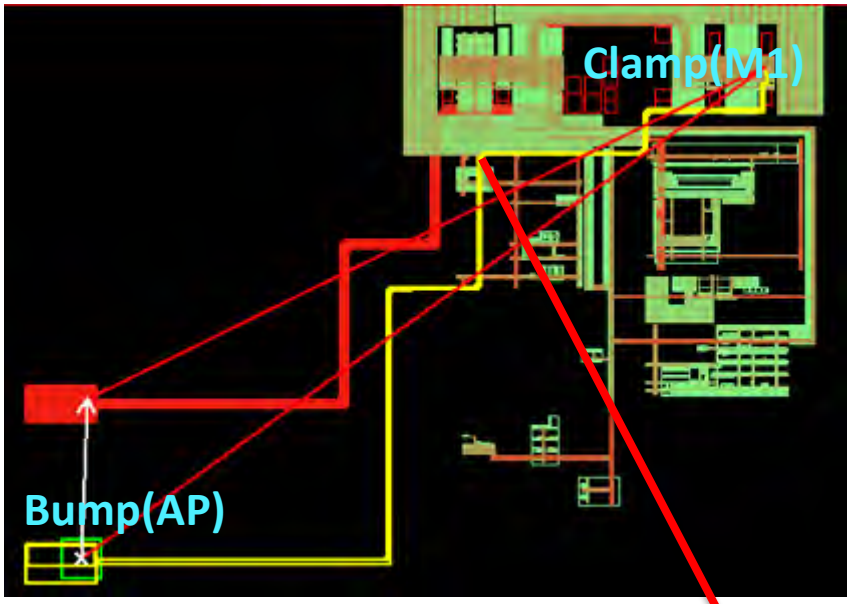
Rule Based RES Check



Resistance check rule :

1. **B2B (Power pad to Ground pad) < 1 Ohm**
2. **B2B (Signal pad to Power pad) < 1 Ohm**
3. **B2B (Ground pad to Signal pad) < 1 Ohm**
4. **B2B (Ground1 pad to Ground2 pad) < 1 Ohm**
5. **C2C (Diode to Clamp) < 1 Ohm**

Analogix R Check Case



B2BM pad_r_sw_Def -> AVDD18_PLL_Def (1-1)

	Point	Layer	Res(Ohm)	ResDiff	Volt(mV)	VoltDiff
1	(1129.095 , 4391.6...	M1	11.687	–	0.000	–
2	(1131.465 , 4381.6...	M1	11.687	0.000	0.000	0.000
3	(1131.465 , 4371.9...	M1	9.560	2.127	98.013	-98.013
4	(1130.815 , 4370.2...	M1	6.082	3.478	113.529	-15.516
5	(1130.815 , 4370.2...	M2	5.734	0.348	115.647	-2.119
6	(1130.815 , 4370.2...	M3	5.386	0.348	120.117	-4.470
7	(1130.815 , 4370.2...	M4	4.853	0.533	129.796	-9.679
8	(1130.815 , 4370.2...	M5	4.320	0.533	139.298	-9.502
9	(1130.815 , 4370.2...	M6	3.786	0.533	149.122	-9.824
10	(1130.905 , 4370.2...	M6	3.776	0.010	149.592	-0.470
11	(1130.905 , 4370.2...	M7	3.726	0.050	154.668	-5.076
12	(1129.785 , 4370.2...	M7	3.720	0.006	155.084	-0.416
13	(1126.690 , 4369.1...	M8	3.711	0.008	161.984	-6.900
14	(1126.690 , 4337.6...	M8	3.627	0.084	223.608	-61.624
15	(980.110 , 4337.665)	M8	3.117	0.509	767.446	-543.838
16	(980.110 , 4334.665)	M8	3.108	0.009	770.852	-3.406
17	(981.485 , 4333.415)	M8	3.099	0.009	773.620	-2.768
18	(979.735 , 4329.915)	M8	3.091	0.008	783.963	-10.342
19	(979.360 , 4326.165)	M8	3.080	0.010	797.242	-13.280

AP => M1

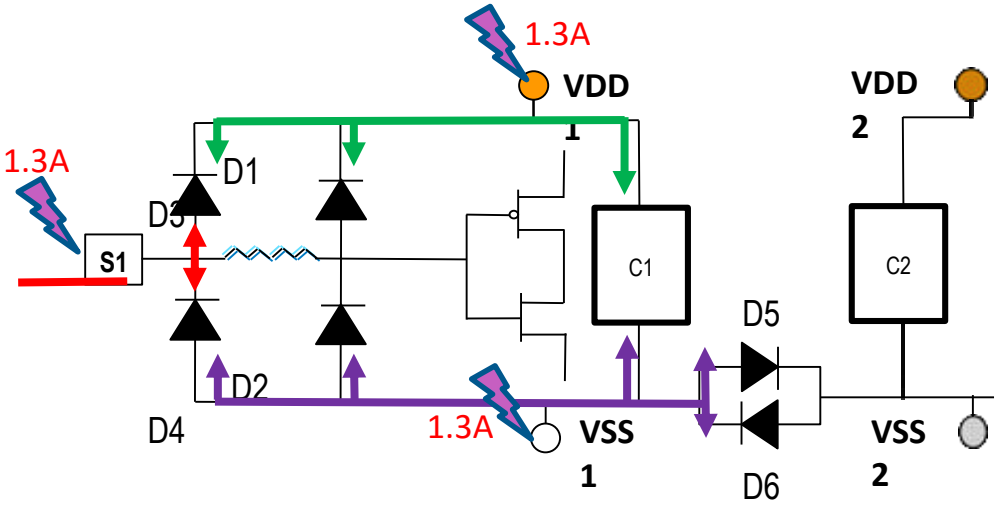
R↑

Min-res arc for this Bump have 3.2ohm res, bigger than the B2C_R threshold 0.5ohm

The long routing from Bump to Clamp cause high resistance

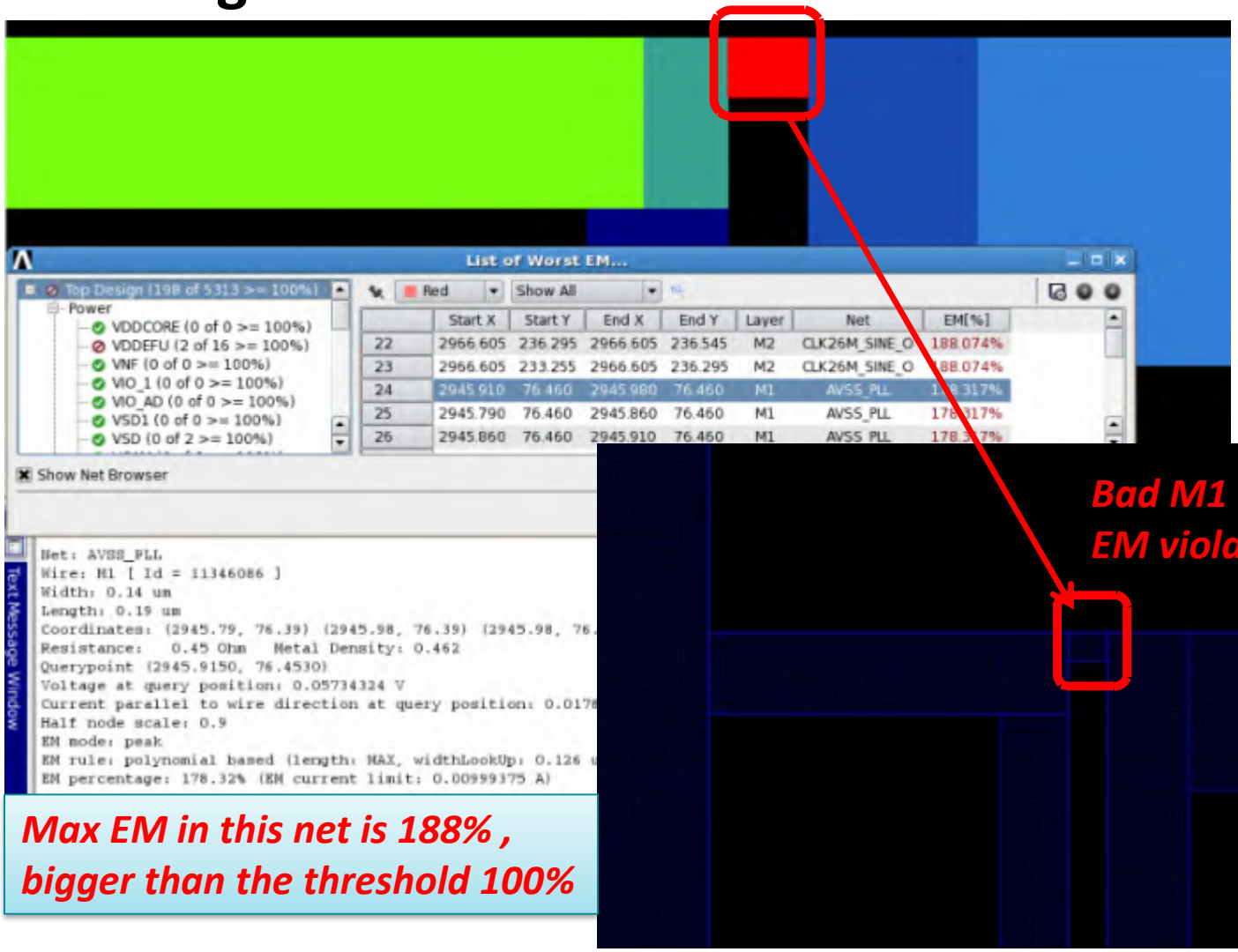
Use short path trace(SPT) utility to highlight the min-res path from the Bump to the selected clamp

Rule Based CD Check



Current Density check rule :
1. Bump2Clamp check: from All pad to corresponding Clamp/Diode zap 1.3A current

Analogix CD Check Case

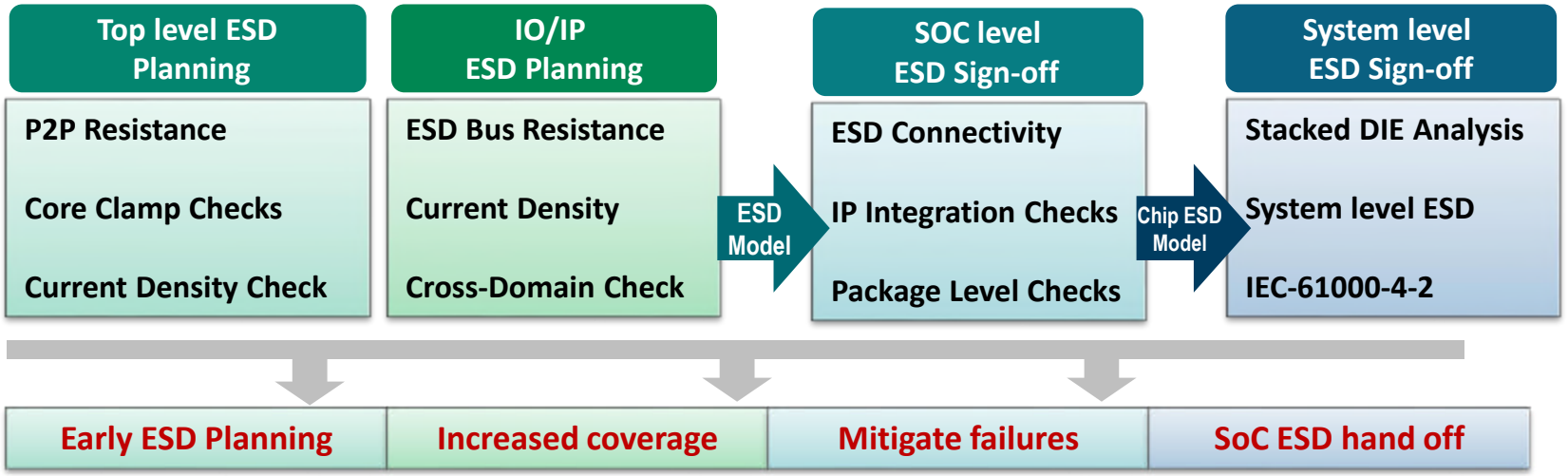


Performance Summary

STAGE		WALL TIME	MEMORY USAGE(GB)
GDS2DB		42mins	49
Setup Design + Extraction		2 hour 56 mins	73
Resistance Check	Bump to Bump Check (All ARCs)	3hour 10 mins	79
	Clamp to Clamp Check (Diode to Clamp)		
Current Density Check	Bump to Clamp Check(All ARCs)	2 hour 20 mins	103

**this performance are got without any reduction in design or metal geometries.*

PathFinder: Full chip ESD Integrity Sign-off



ESD Integrity Verification and Sign-off with PathFinder

感谢聆听