



ANSYS中国技术大会
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从芯片到系统ESD静放电分析

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引言

- 对于现代电子产品而言，ESD属于关键设计，并且有明确的安全规范（IEC61000-4-2或GB/T 17626），尤其是对于MP3、数码相机、摄像机和手机等便携式设备。当电子设备发生ESD时，产品内部的PCB上会产生感应电流，导致设备发生故障。大部分电路和系统设计工程师使用硬件测试和调试等手段解决ESD问题。然而，这种方式需要多次设计迭代，增加开发成本。一种合适的方式是通过软件仿真的手段将ESD解决过程转移到设计早期。软件仿真可帮助电路和系统设计工程师快速评估ESD防护性能，从多种设计方案中筛选出最佳设计。ESD防护仿真有两种方式：一种为纯电磁场分析，评估ESD放电区域和瞬态感应电场分布。另一种为电磁场和电路协同分析，快速准确的评估和优化ESD防护设计，以及对其他信号的影响。
- ANSYS公司利用其专业电磁场和电路仿真工具相互协同，通过动态链接和激励推送构成的双向耦合，为用户提供完善的从芯片到系统的ESD仿真平台。在此平台上，用户可以参照评估包括芯片/封装、连接器、PCB电路板和外壳等复杂系统中的ESD静放电现象，检查设计中的ESD隐患，评估ESD防护电路和放电之后的电磁能量分布。


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Objectives

- CPS ESD Simulation Methodology addressing IEC61000-4-2 testing conditions**
 - Provide a realistic view of voltage/current versus time on the chip pins through accurate modeling and simulation of the CPS ESD prior to hardware availability
 - Perform diagnosis of potential failure mechanisms when CPS ESD failures occurred
 - Verify robustness of an ESD fix by comparing differential voltage/current values against maximum safe thresholds on the IC chip(s) pins with hard or soft failure
- examples of CPS ESD application are illustrated demonstrating good correlation with measurement**

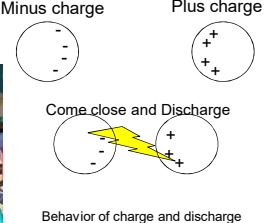

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Electrical Static Charge(ESD)

- Electrostatic is phenomenon that charged body take on electric charge and discharge electricity.
- Plus and minus charged body come near together, gas between them ionize, after that electricity goes through ionized gas to another charged body. Ionized condition depend on degree of humidity, temperature, dust and EM condition. This condition does not only define EM condition.
- Role of EM simulator**
 - ✓ Behavior of electric charge before discharge
 - ✓ Current route and strength after discharge



Electric static charge phenomenon



Behavior of charge and discharge

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Confirm a place of strong electric charge, electric field

- Set difference of voltage between hand and mobile phone in a model, check behavior of electric charge and electric field
 - This results show us a place of possibility of discharge.
 - On the Q3D result, it show us that metal area ABS_Q is red, it speaks for metal avoid discharging to board which IC is mounted on.

Human hand and Cellular phone Charge density(absolute value) (Q3D) Static electric field (Maxwell3D)

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Confirm conduction current after discharge

- Analyze PCB which is 2 different GND shape condition PCB under below conduction route(blue arrow)
 - Surface layer: signal, Back layer: all GND plane
 - Connector is set on GND edge
 - On the HFSS-Transient result, Conduction current is from connector GND edge to PCB GND edge(red arrow)
- Left model does not have GND shield, as result, strong current density area is near center PCB.(red circle)
- Right model has GND shield, this avoid current inflowing.(red circle)

Input Current from Connector GND edge Break away current from PCB GND edge Conduction route PCB with USB connector

None shield Add shield with via to 2mm offset from PCB edge PCB with surface shield

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Dynamic link Circuit and EM Field

- Pulse wave shape from Electric gun is constituted on IEC61000-4-2 EMC regulation.
- If we estimate noise from gun on board with circuit simulator, it is easy to take steps for better design.

Gun_Source Voltage pulse shape from electric gun

Apply noise from electric gun to PCB on Cellular phone.

3D model Confirm noise behavior on PCB under operation

HFSS EM analysis + Nexxim Transient analysis

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Outline

- Modeling for CPS ESD Simulation**
 - Chip ESD Compact Model
 - ESD Gun Zap Modeling
 - Full 3D FEM ESD Gun
 - TVS Protection Devices Modeling
 - TVS Diodes, CMF/EMI/ESD Filter
 - PCB and Connector Modeling
 - Mobile PCB, Micro USB Connector
- Application Examples**
 - Case Study : Mobile System-level ESD Propagation Modeling
 - Predict Chip pin $V(t)/I(t)$, ESD Propagation Prediction
 - Correlation with Measurement

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System-level ESD Testing

• The Mobile system ESD test platform that incorporates all major components of a converged Device that need to be modeled for simulation

- Chip/Package
- PCB, Connectors
- Housing
- Battery
- Components
- Etc...

Current waveforms of an ESD generator

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Where to Apply ESD 哪里应用ESD设计才有效

Shielding 设备屏蔽 OK	Board filtering PCB板滤波 Better	IC and Board design 芯片和板设计 Best

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ESD Issues on PCBs 板级ESD问题

□ Issues

- Mobile product 移动设备
 - ▶ Lacking of ground 缺少接地
- Tighter noise margin 噪声敏感的环境
 - ▶ IC sensitivity 芯片敏感度高
- High density and small size PCB 高密度小尺寸PCB
 - ▶ Physically close to port/chassis 物理上接近接口或机壳
- the number of I/F port 接口多
 - ▶ Easily exposed to ESD event 容易暴露在ESD环境下

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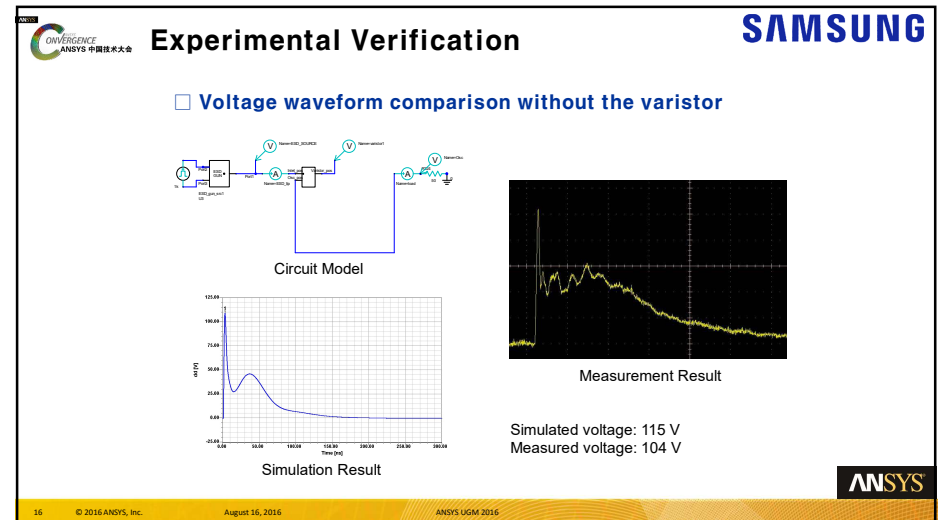
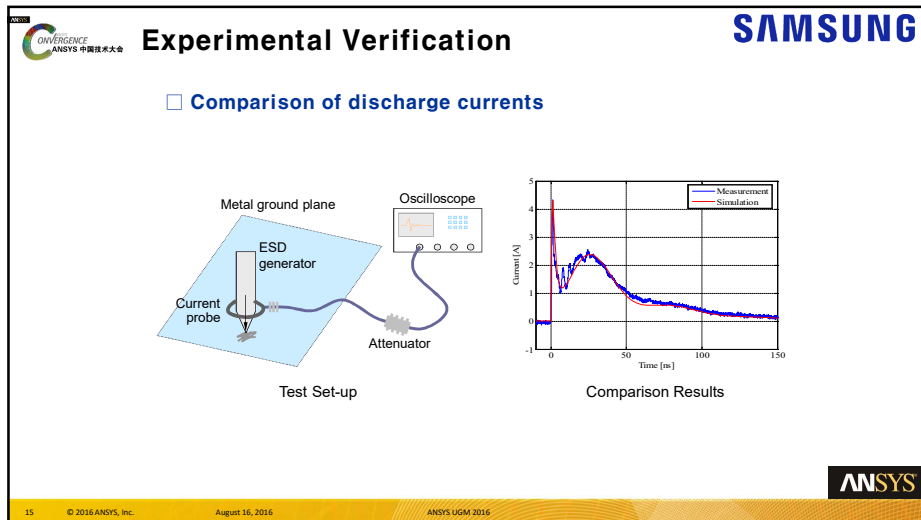
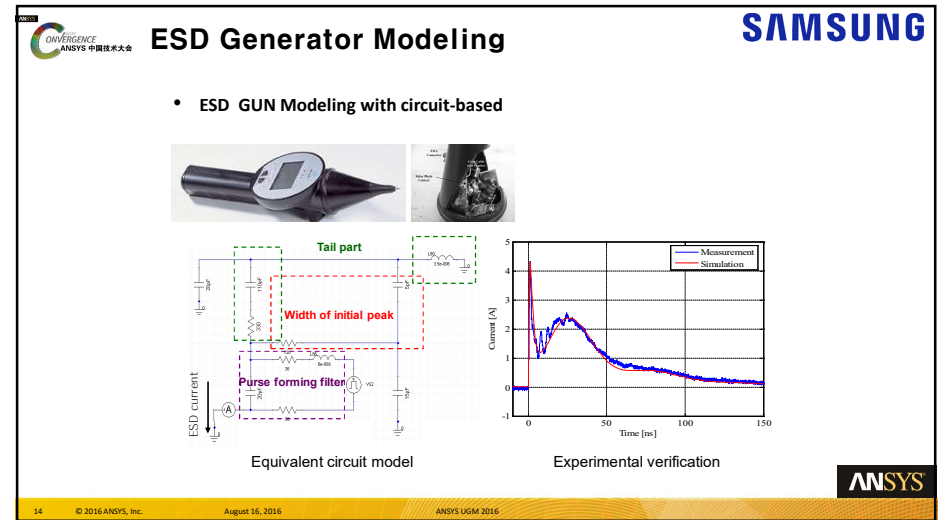
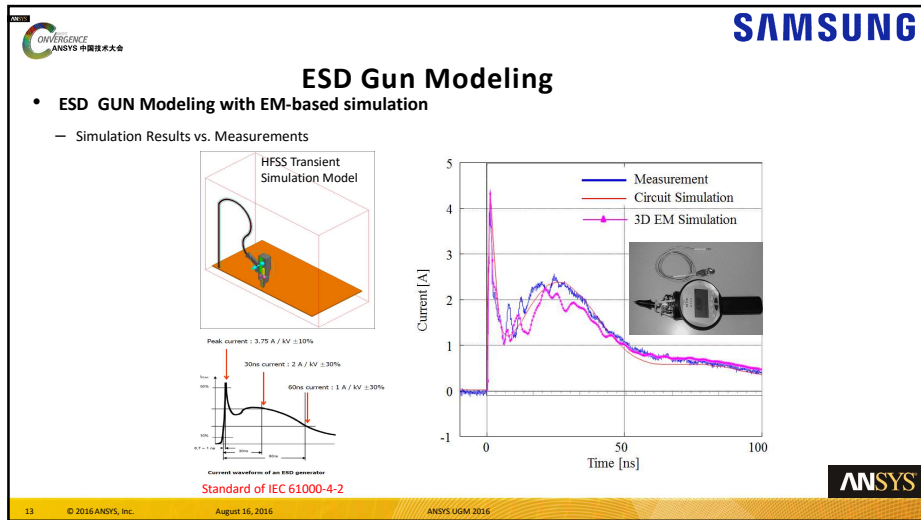
Chip ESD Compact Model for ESD Simulation

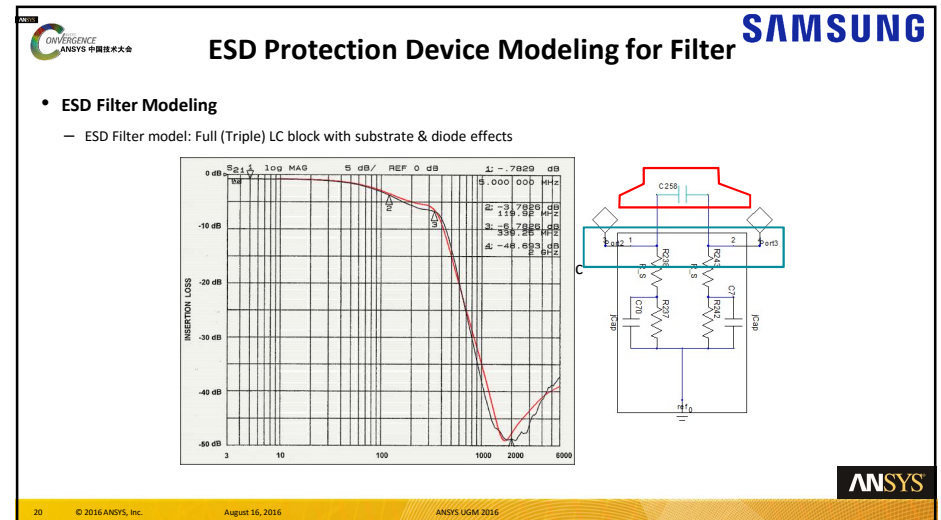
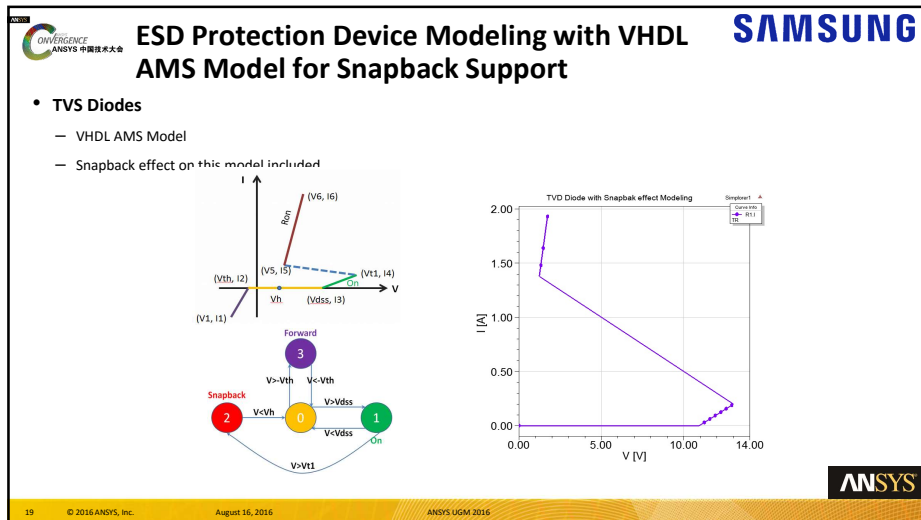
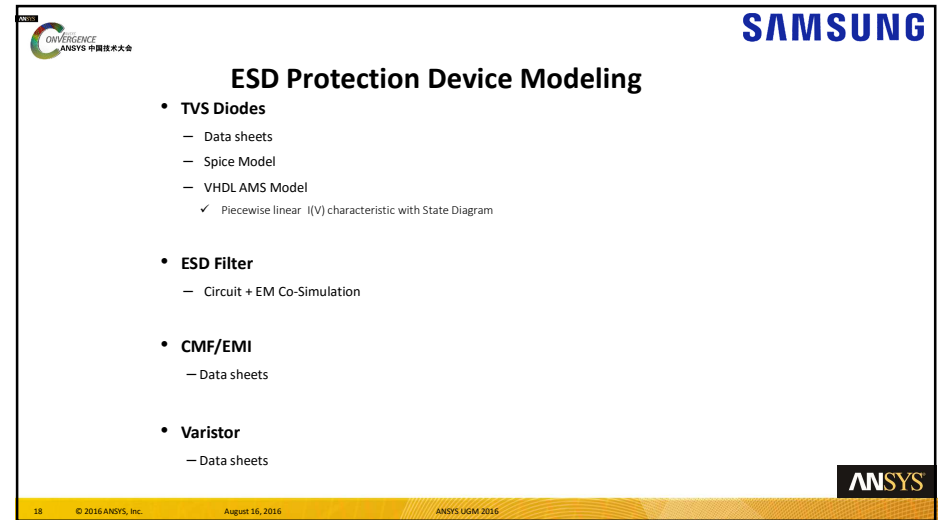
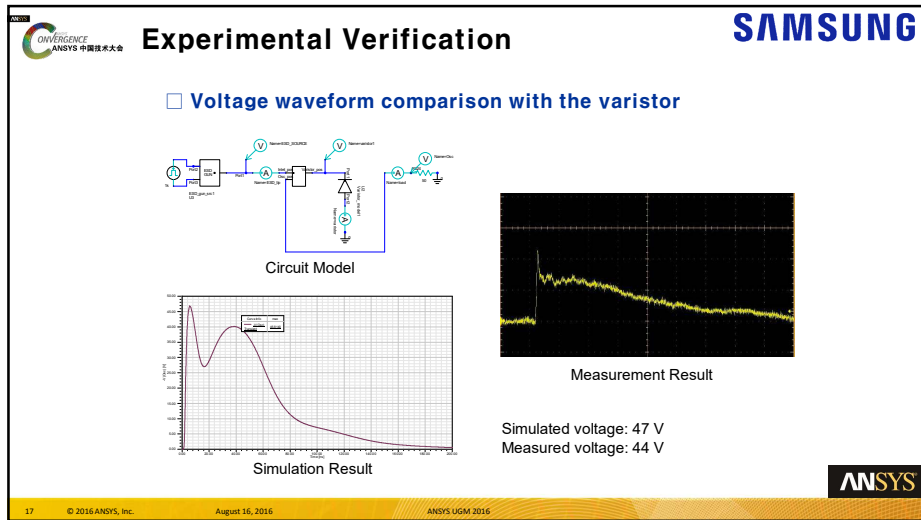
• Chip ESD Compact Model

- Chip ESD Compact Model (CECM) provides a reduced and distributed RLC network among ports and per port demanding current for the chip power-on status with a chosen chip operation vector
- On-chip decaps are modeled including intrinsic device decap, power/ground cap, intentional decap, and effective loading cap
- On-chip diode/clamp I-Vs can be included in the model when generating from Pathfinder-S which is an on-chip ESD analysis tool

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ESD Protection Device Modeling For CMF/EMI Filter

CMF/EMI Filter Modeling

- Data sheets
- Single-ended equivalent model for common mode (Simple approximation)

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ESD Protection Device Modeling for Varistor

Test set-up

V_s : pulse source voltage
 R_s : pulse source impedance (50ohm)
 R_t : termination resistance of scope (50ohm)
 V_c : clamping voltage on varistor
 I_v : current flowing on varistor for given clamping voltage
 R_v : resistance of varistor for given clamp voltage

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ESD Protection Device Modeling for Varistor

Voltage and current characteristics for the varistor

The non-linear resistance characteristic of the varistor can be expressed in exponential function as:

$$I_v = KV_c^\alpha$$

V_s (V)	V_c (V)	R_v (Ω)	I_v (A)
88	35	97.22	0.36
190	40	18.18	2.20
270	43	11.68	3.68
360	45	8.33	5.40

Measure V_c on the oscilloscope
 Calculate $R_v = (50 \times V_c) / (V_s - 2 \times V_c)$
 Calculate $I_v = V_c / R_v$
 $\alpha = \log(V_{c2}/V_{c1}) / \log(I_{v2}/I_{v1})$
 $I_v = 1.47 \times 10^{-12} V_c^{7.6}$

Voltage vs. current for the varistor

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ESD Protection Device Modeling for Varistor

SPICE model and simulation

The non-linear device can be modeled using voltage controlled current source

非线性器件模型可以用压控电流源来建模

Simulated voltage and current characteristics for the varistor (derived from the equation;
 $I_v = 1.47 \times 10^{-11} V_c^{7.6}$)

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PCB Modeling

☐ Circuit model integrating a PCB with the ESD generator

Test board

Port: ESD injection

Port: Oscilloscope

Simulation model using Siwave

FWS → Export to Designer

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Full Circuit Model

☐ Combined circuit model

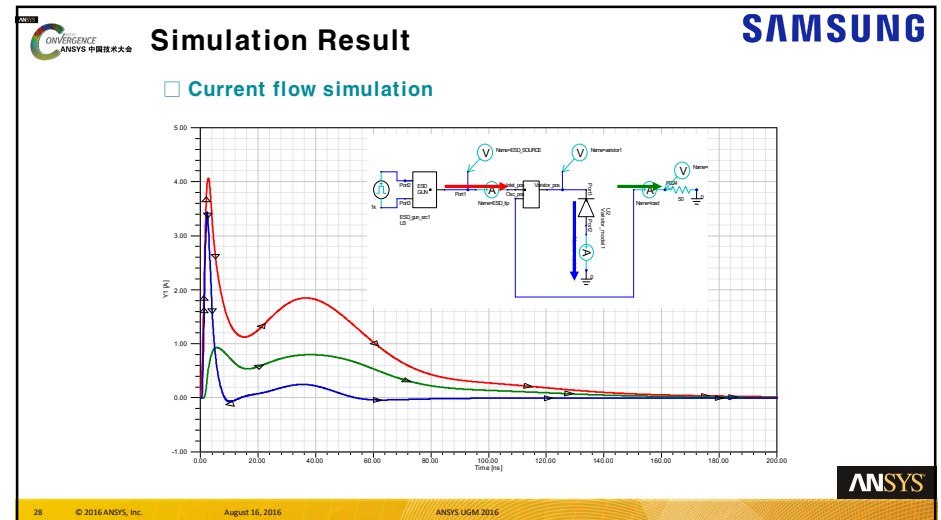
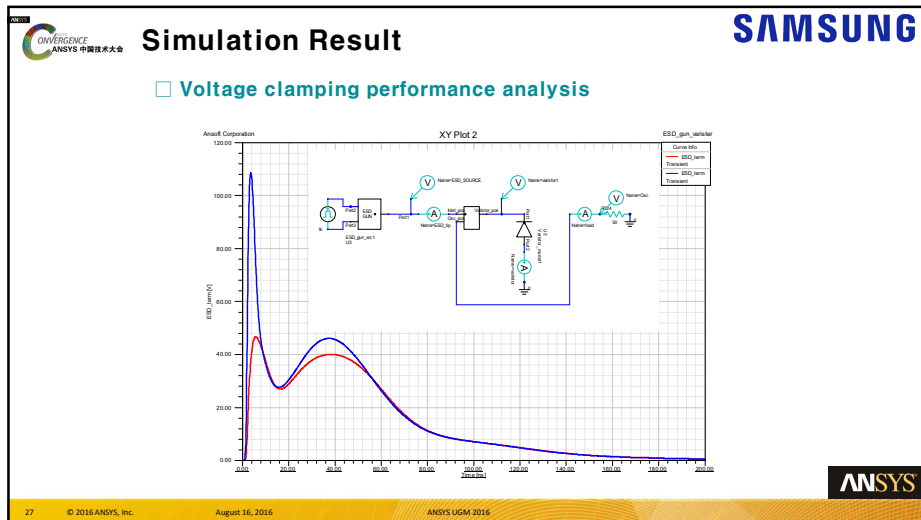
ESD generator

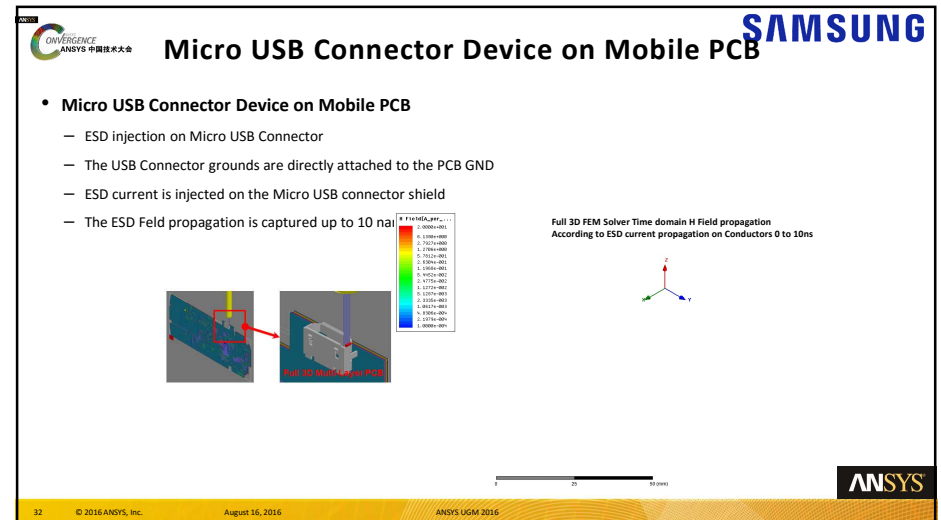
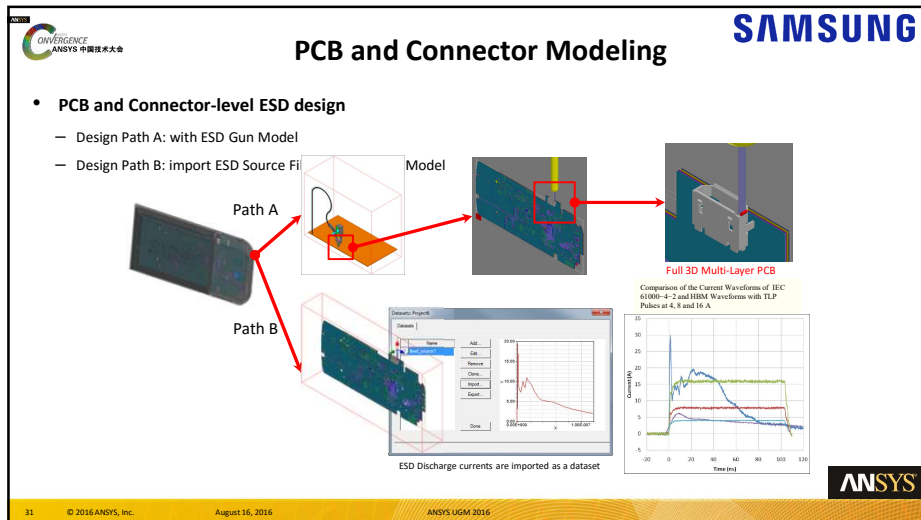
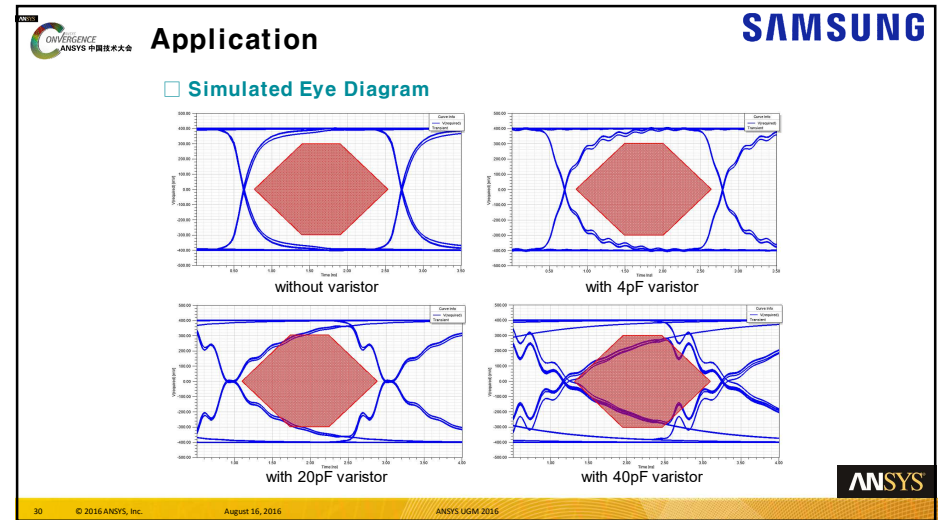
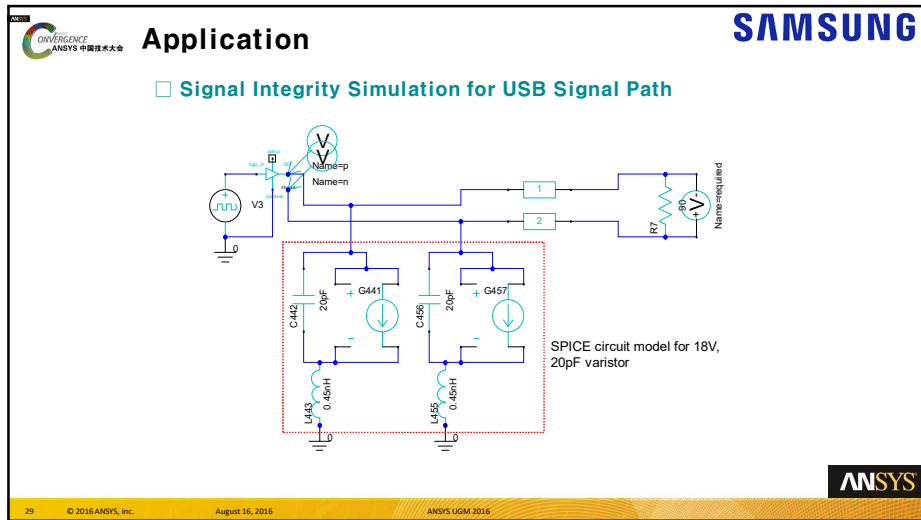
Printed circuit board

Varistor

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System-level ESD Propagation Modeling **SAMSUNG**

- System-level ESD propagation modeling for Mobile Device

VBAT, VCC1.2v, VCC1.8v, VCC2.9v, VCC3.3v, VAP's & Memory Power, VUSB And Ground

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System-level ESD Propagation Modeling - I **SAMSUNG**

- System-level ESD propagation modeling for Mobile Device

Typical implementation of a USB2 interface

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System-level ESD Propagation Modeling - II **SAMSUNG**

- Mobile System-level ESD propagation modeling
 - 5kV ESD Injection on Micro USB Connector

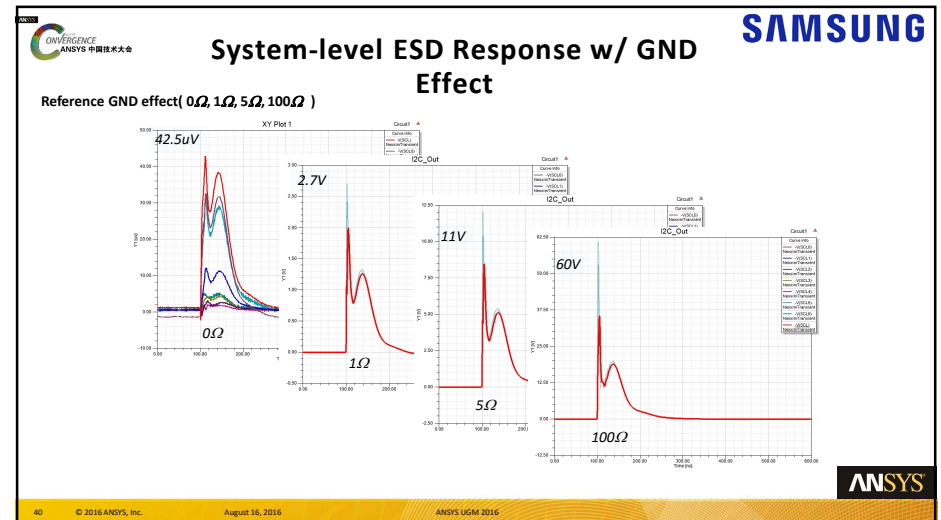
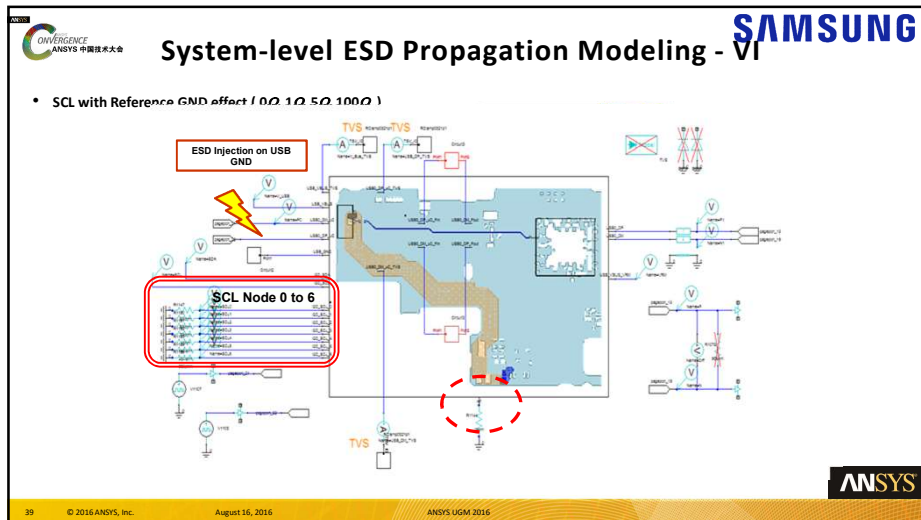
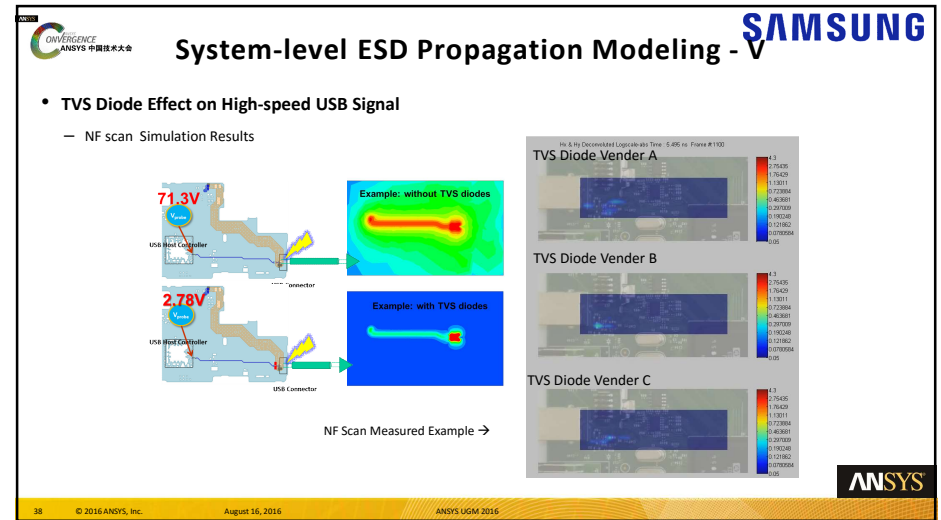
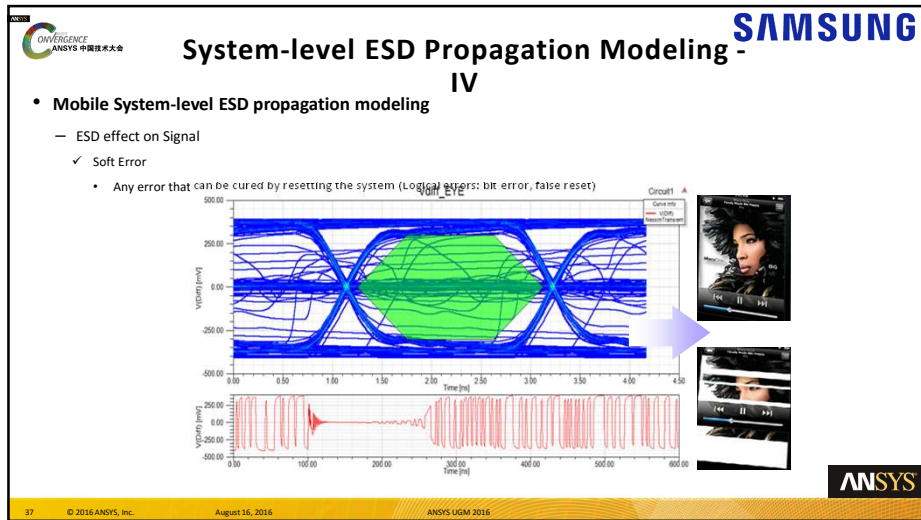
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System-level ESD Propagation Modeling - III **SAMSUNG**

- Mobile System-level ESD propagation modeling
 - Easy to perform "What if" studies
 - Contact vs. Air Discharge
 - Discharge

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System-level ESD Propagation Modeling

- Mobile system-level ESD propagation modeling
 - Outline a comprehensive Chip-Package-System ESD simulation methodology that particularly addresses the interface modeling between the ESD gun and system, and the interface modeling between the system and IC chip(s) are very important.

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System-level ESD Response w/ Different Cdie

- Chip pin V(t) response w/ different Cdie
 - Chip pin V(t) response with different chip Cdie to provide guidance on the effectiveness of ESD protection on PCB (or system)

Curve Info	max
VESD_on_IC_inpad	9.9141
Transist	9.9141
Cdie=20pF	6.9659
VESD_on_IC_inpad	3.4166
Transist	3.4166
Cdie=30pF	2.5779
VESD_on_IC_inpad	2.0700
Transist	2.0700
Cdie=40pF	

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Experimental Verification

- Test board and Measurement setup

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Conclusions

- Comprehensive CPS modeling and simulation for IEC61000-4-2 testing conditions
 - "Frequency dependent component such as Common Mode Filter & TVS Diode with I-V characteristics" can be modeled and used as a part of system-level ESD simulation
 - Chip pin V(t) and I(t) curve are identified through CPS simulation with distributed RLC, port current modeling, and optionally diodes/clamp I-Vs in CECM Model
 - 3D FEM solver provides the robustness in analyzing transition of spike current with visualization
 - Dynamic link circuit and EM field to evaluate ESD protection easily
- Many examples of CPS ESD application are illustrated demonstrating good correlation with measurement
 - ESD zap gun measurement result correlates well with simulated zap current waveform
 - Voltage waveform correlated well between measurement and simulation on a test board measurement setup

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